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Subject Name: Basic Electronics	Faculty: Tejashree S
Subject Code: BBEE103/203	Scheme: 2022

Syllabus:

Bipolar Junction Transistors: Introduction, BJT Voltages & Currents, BJT Amplification, Common Base Characteristics, Common Emitter Characteristics, Common Collector Characteristics, BJT Biasing: Introduction, DC Load line and Bias point.

Field Effect Transistor: Junction Field Effect Transistor, JFET Characteristics, MOSFETs: Enhancement MOSFETs, Depletion Enhancement MOSFETs.

Introduction:

- A transistor is a semiconductor device that controls current with the application of a small electrical signal.
- Transistors may be roughly grouped into two major families: bipolar and field-effect. BJT utilize a small current to control a large current. But, FET utilizing a small voltage to control current.
- FETs are unipolar rather than bipolar devices. That is, the main current through them is comprised either of electrons through an N-type semiconductor (N-channel FET) or holes through a P-type semiconductor (P-channel FET).
- In a JFET, the controlled current passes from Source to Drain, or from Drain to Source as the case may be. The controlling voltage is applied between the Gate and Source. Current flowing through this channel widely depends on the input voltage applied to its Gate terminal.
- FETs generally of two types: 1) JFET (Junction Field Effect Transistors) and 2) MOSFET (Metal Oxide Semiconductor Field Effect Transistors).

Junction Field Effect Transistors: JFET is a voltage controlled three terminal uni-polar semiconductor device. The three terminals namely, Source (S), Gate (G) and Drain (D).

As the voltage applied to the Gate with respect to the Source (VGS), controls the current flowing between the Drain and the Source terminals. See fig.2.1. JFETs can be classified into two types (i) n-channel JFET and (ii) p-channel JFET, depending on whether the current flow is due to electrons or holes, respectively.

Components of FET:

1. **Channel:** This is the area in which majority charge carriers flow. When the majority charge carriers are entered in FET, then with the help of this channel only they flow from source to drain.

2. Source: Source is the terminal through which the majority charge carriers are introduced in the FET.

3. Drain: Drain is the collecting terminal in which the majority charge carriers enter and thus contribute in the conduction procedure.

4. Gate: Gate terminal is formed by diffusion of a type of semiconductor with another type of semiconductor. It basically creates high impurity region which controls the flow of carrier from source to drain.

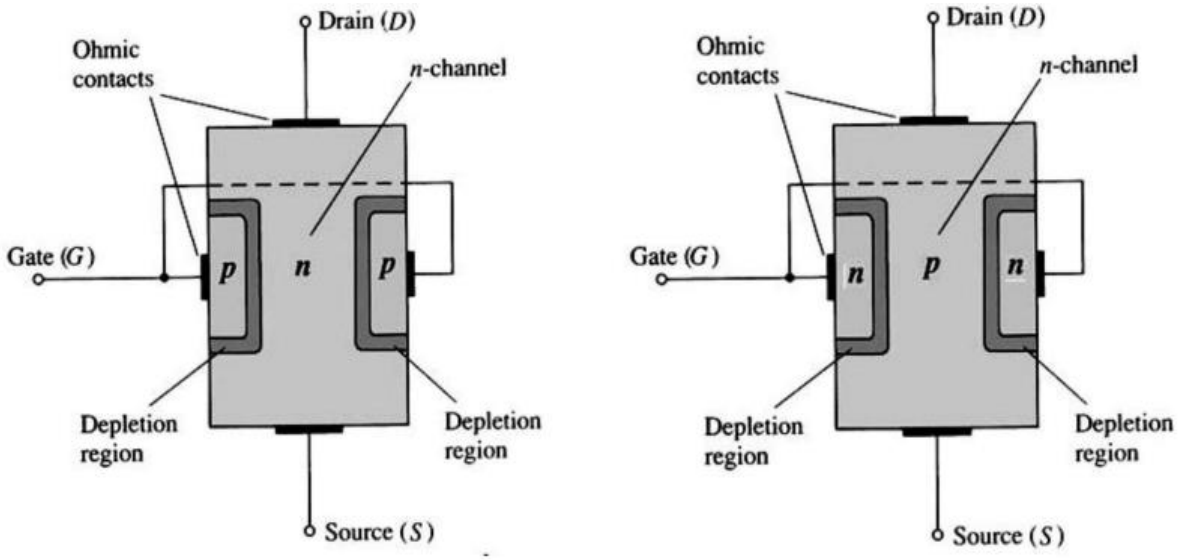


Fig 2.1: Constructional details of a) N-channel JFET b) P-channel JFET

Working of N-channel JFET:

Case I: No voltage is applied to the device (V_{DS} = 0 and V_{GS} = 0).

At this state, the device will be idle and no current flows through it (I_{DS} = 0).

Case-II: When V_{DS} is applied and V_{GS} = 0

As shown in fig.2.2 (a), the two PN junctions at the sides of the N channel establish depletion layers. The electrons will flow from Source to Drain through a channel between the depletion layers. The size of the depletion layers determines the width of the channel and hence current I_{DS}, conduction through the bar.

Case-III: When V_{DS} is applied and V_{GS} = - ve

The depletion region width increases, which results in reduces the width of conducting channel, thereby increasing the resistance of n-type bar. Consequently, the current from Source to Drain is decreased.

If more ($-V_{GS}$) is applied, further reduces the channel width until no current flows through the channel. At this - voltage at which the JFET channel is called as pinched-off voltage, V_P.

At this state, the I_{DS} current is restricted only by the channel-resistance. However, once the pinch-off occurs ($V_{DS} = V_P$), the current I_{DS} saturates at a particular level I_{DSS}.

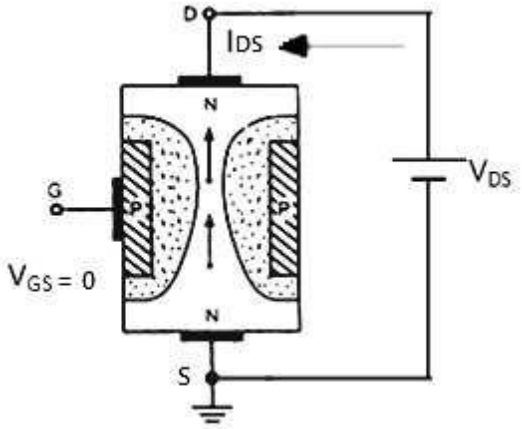


Fig 2.2 (a)

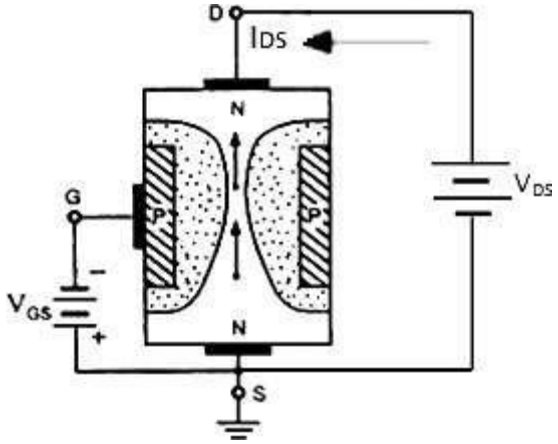


Fig 2.2 (b)

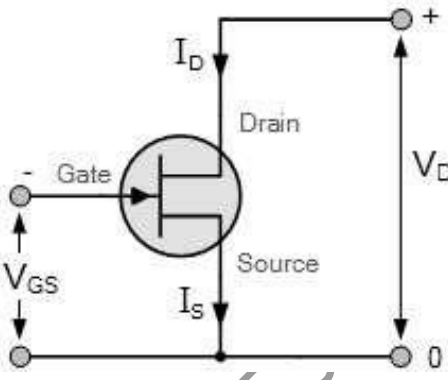


Fig 2.3: Circuit diagram of N-channel JFET

Output characteristics (Drain) V-I curves of JFET:

The characteristics curves of a JFET shown in the fig.2.4, reveals four different regions of operation aregiven as:

- ***Ohmic Region:*** When V_{GS} = 0 the depletion region of the channel is very small and the JFET actslike a voltage controlled resistor.
- ***Cut-off Region:*** This is also known as the pinch-off region were the Gate voltage, V_{GS} is sufficient to cause the JFET to act as an open circuit as the channel resistance is at maximum.
- ***Saturation or Active Region:*** The JFET becomes a good conductor and is controlled by the Gate-Source voltage, (V_{GS}) while the Drain-Source voltage, (V_{DS}) has little or no effect.
- ***Breakdown Region:*** The voltage between the Drain and the Source, (V_{DS}) is high enough to causes the JFET's resistive channel to breakdown and pass uncontrolled maximum current.

The characteristics curves for a P-channel junction field effect transistor are the same as those above, except that the Drain current I_D decreases with an increasing positive Gate-Source voltage, V_{GS}.

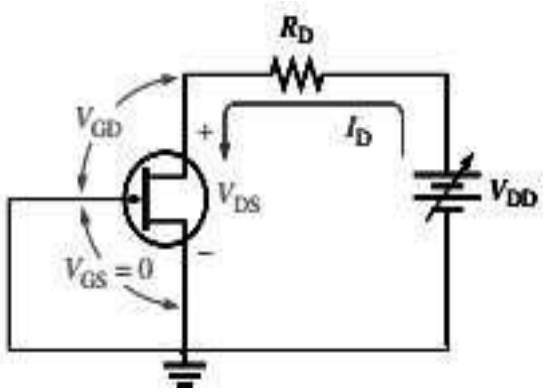
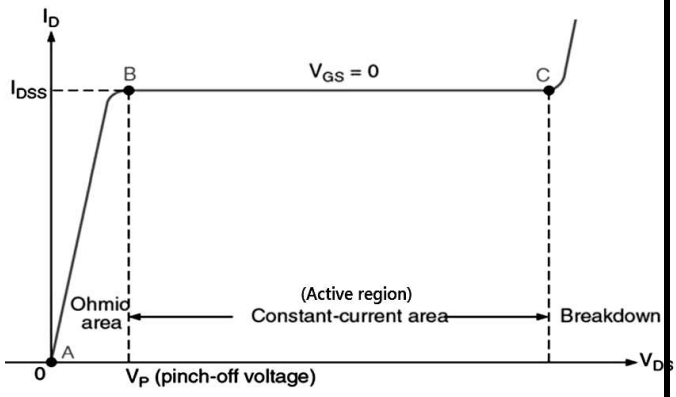


Fig 2.4 (a) JFET with VGS=0V and a variable VDS(VDD)



(b) The drain Characteristics curve for VGS=0 showing pinch off voltage

The Drain current IDS is zero when VGS = VP. For normal operation, VGS is biased to be somewhere between VP and 0. Then we can calculate the Drain current, ID for any given bias point in the saturation or active region as follows:

1. ***Drain current in the Active region:***

   Drain current (I_D) at the active region can be calculated as follows: I_D lies between (pinch-off) zero to I_{DSS}.

$$I_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2$$

2. ***Drain-Source Channel Resistance R_{DS}:***

   Similarly, if we know drain source voltage Vds and drain current Id, we can calculate the drain-source channel resistance.

$$R_{DS} = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1}{g_m}$$

Where: gm is the "trans conductance gain" since the JFET is a voltage controlled device and which represents the rate of change of the ID with respect to the change in VGS.

3. ***Amplification Factor: (μ)***

   It is given by

$$\mu = \frac{\text{change in } V_{DS}}{\text{change in } V_{GS}} \text{ at } I_D \text{ constant}$$

Transfer characteristics of JFET:

The transfer characteristics can be determined by observing different values of I_D with variation in V_{GS} provided that the V_{DS} should be constant as shown in the fig.2.5.

Notice that the bottom end of the transfer characteristic curve is at a point on the V_{GS} axis equal to $V_{GS}(off)$, and the top end of the curve is at a point on the I_D axis equal to I_{DSS}.

This curve shows that

i) ID = 0; when VGS = VGS(off)

ii) ID = IDSS when VGS = 0

iii) The transfer characteristic curve is expressed approximately as

$$I_D \cong I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

Hence, JFETs are often referred to as square-law devices.

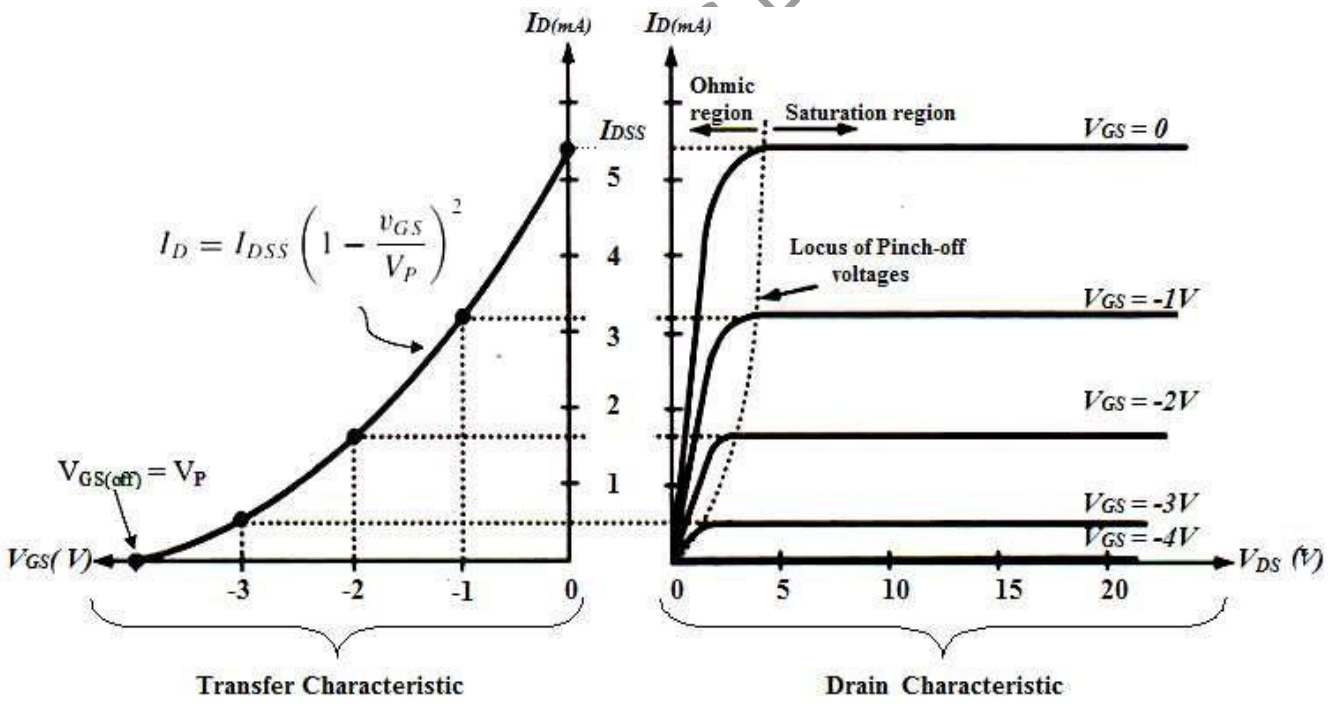


Fig 2.5 Transfer and Drain characteristics

Comparison of BJT and FET:

BJT	JFET
Bipolar junction transistor	Unipolar junction transistor
Input impedance is very less	Input impedance is very large
Current control device, preferred for low current applications	Voltage controlled device, preferred for low voltage applications
More noisy	Less noisy
Frequency variations effect its performance	High frequency response
Temperature dependent device	Better heat stability
Cheaper than FET	Costly than BJT
Bigger in size than FET	Smaller in size than BJT
More gain	Less gain
High output impedance because of high gain	Low output impedance because of less gain
High voltage gain	Low voltage gain
Low current gain	High current gain
Switching time is medium	Switching time is fast
Consumes more power	Consumes less power

Metal Oxide Semiconductor Field Effect transistor (MOSFET):

- The MOSFET, different from the JFET, has no *pn* junction structure; instead, the gate of the MOSFETis insulated from the channel by a silicon dioxide (SiO2) layer shown in the fig.2.6.

- The MOSFET is widely used for switching and amplifying electronic signals. Also, it is a core of ICs and it can be designed and fabricated in a single chip because of smaller silicon chip area.

The two basic types of MOSFETs

1. Enhancement MOSFET (E-MOSFET) and
2. Depletion MOSFET (D-MOSFET). Of the two types, the enhancement MOSFET is more widely used.

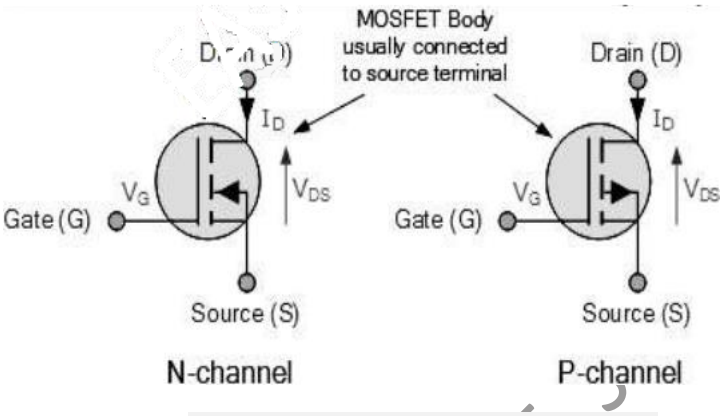


Fig.2.6 MOSFET circuit symbols

The depletion mode MOSFETs are generally ON at (V_{GS} = 0V). The conductivity of the channel in depletion MOSFETs is less compared to the enhancement type of MOSFETs. See fig. 2.7.

Case I: When there is no Gate voltage (V_{GS} = 0), as in fig. 2.7, maximum current flows ($I_D = I_S = I_{DSS}$).

Case II: When V_{GS} = -ve with respect to the substrate, the Gate repels some of the electrons out of the N-channel.

This creates a *depletion region* in the channel, as illustrated in fig.2.8, and, therefore, increases the channel resistance and reduces the Drain current, I_D. The more negative the gate, the less the Drain current.

In this mode of operation, the device is referred to as a *depletion-mode MOSFET.* Heretoo much negative Gate voltage can pinch-off the channel. Then device is said to be OFF.

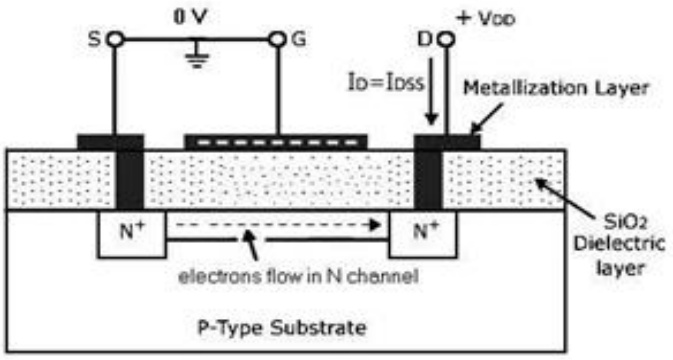


Fig.2.7 MOSFET in depletion mode with gate voltage zero

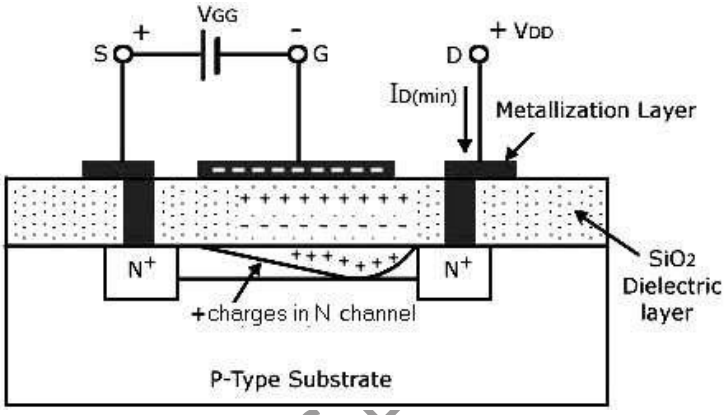


Fig.2.8 MOSFET in depletion mode with gate voltage negative

Case III: When V_{GS} = +ve, Gate attracts the negative charge carriers from the P-substrate to the N- channel and thus reduces the channel resistance and increases the drain current, I_D. The more positive the Gate is made, the more Drain current flows. In this mode of operation, the device is referred to as an enhancement-mode MOSFET. This is depicted in the fig. 2.9.

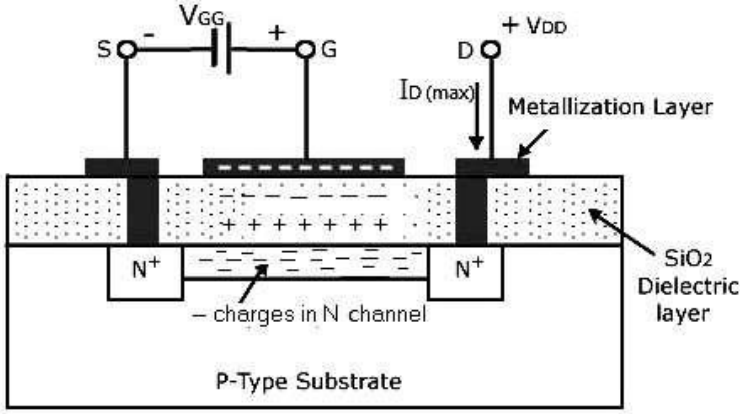


Fig.2.9 MOSFET in depletion mode with gate voltage positive

Transfer and Drain characteristic of depletion MOSFET is shown in the fig.2.10.

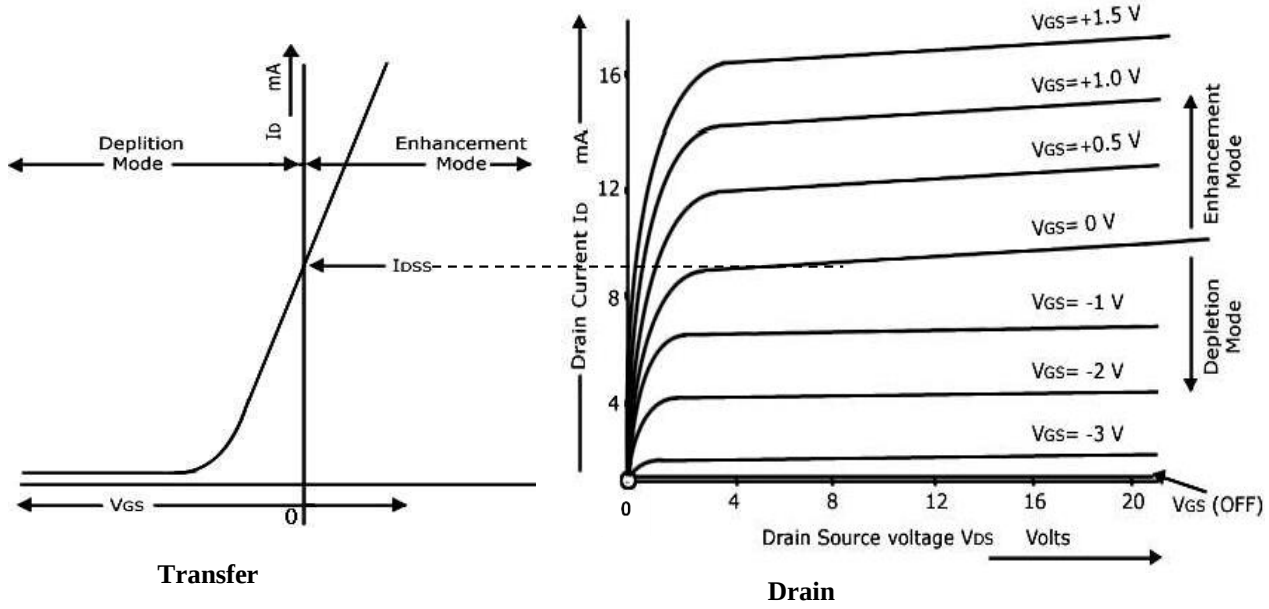


Fig. 2.10 Transfer characteristic and Drain characteristic of depletion MOSFET

Enhancement Mode:

The construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of an N-channel between the drain and source terminals.

The minimum value of V_{GS} is required to form the induced N-channel, that turns the E-MOSFET ON is called threshold voltage [$V_{GS\ (th)}$]. For V_{GS} below $V_{GS\ (th)}$, the drain current $I_D = 0$.

(i) **When V_{GS} = 0 V, V_{DS} = +ve:** There is no channel induced between Source and Drain. The p- substrate has only a few thermally produced free electrons (minority carriers) so that drain current is almost zero. For this reason, E-MOSFET is normally OFF when V_{GS} = 0V.

(ii) **When V_{GS} = $V_{GS(th)}$ = + ve, and V_{DS} = + ve:** The free electrons developed next to the SiO2 layer and induced an N channel, as shown in the fig.2.11. Now a Drain current I_D starts flowing. E-MOSFET is turned ON. Beyond $V_{GS\ (th)}$, if the value of V_{GS} is increased, the induced N channel becomes wider, resulting large I_D. If the value of V_{GS} decreases not less than $V_{GS\ (th)}$, the channel becomes narrower and I_D will decrease.

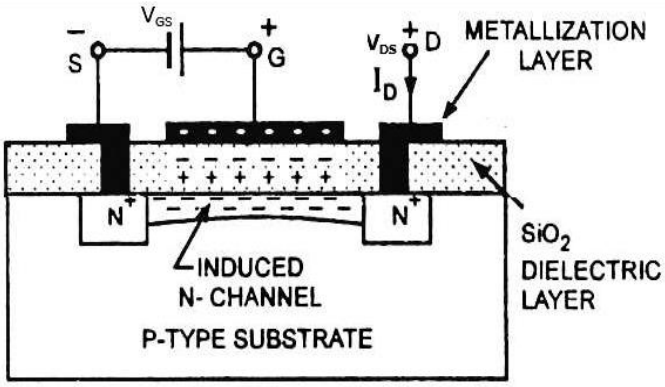


Fig. 2.11 MOSFET in enhancement mode with gate voltage positive

Since the conductivity of the channel is enhanced by the positive bias on the Gate, so this device is also called the enhancement MOSFET or E- MOSFET.

Characteristics of E-MOSFET:

Drain Characteristics curve: fig.2.12 (b), have almost vertical and almost horizontal parts. The vertical components of the curves correspond to the *ohmic region*, and the horizontal components correspond to the *saturation region* (constant current). Note the following worthy points:

- I_D depends on different values of V_{GS} (from 0V to + $V_{GS\ (max)}$).
- When V_{GS} = 0, even for large increase in V_{DS}, I_D = 0. This is said to be cut-off region. (MOSFET *off state*).

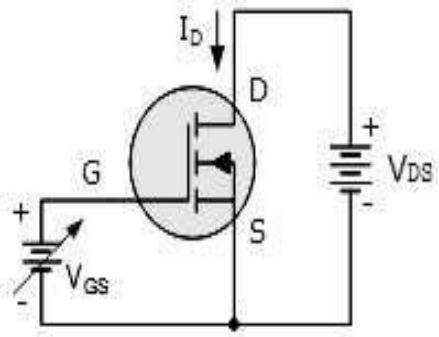
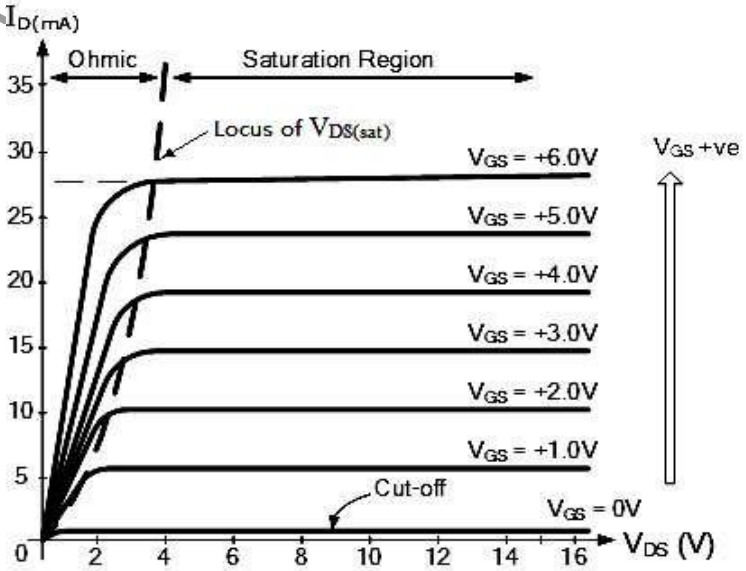


Fig. 2.12 (a) E-MOSFET circuit



(b) Drain characteristic of E-MOSFET

Transfer Characteristics curve:

i. When $V_{GS} < V_{GS(th)}$, then $I_D = 0$. This is because under this state, the channel will not be connecting between the drain and the source terminals. This is called as *cut-off region*. (MOSFET off state). The tranfer curves of MOSFET is shown in the fig.2.13.

ii. When $V_{GS} > V_{GS(th)}$,. then I_D flows through the device, initially (Ohmic region) and then saturates to a value (*saturation region*). That means, I_D is controlled by the Gate voltage, V_{GS}.

iii. I_D can be obtained by analytical expression:

$$I_D = k\,(V_{GS} - V_{GS(th)})^2$$

where $k = \dfrac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$ A/V²

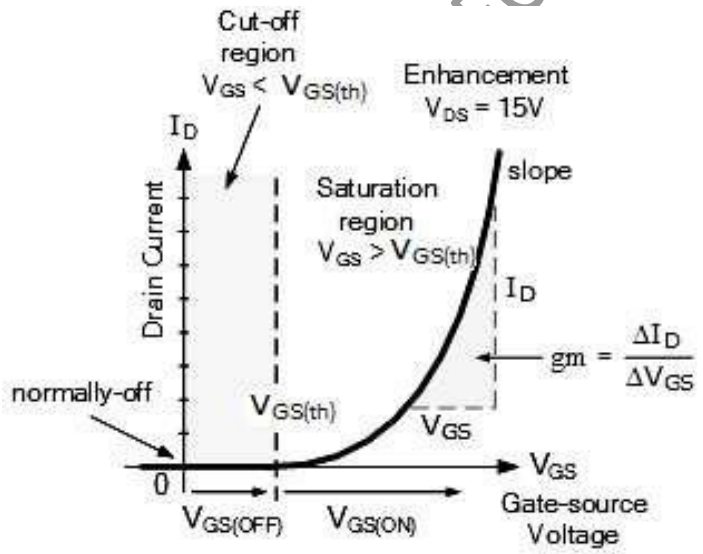


Fig.2.13 Transfer characteristic of E - MOSFET

BBEE13.
Basic Electronics

MODULE-2.
BJT and FET

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Syllabus:

Bipolar junction transistors: Introduction, BJT Voltages and Currents, BJT Amplification, Common Base, Common Emitter, common collector characteristics, BJT Biasing: Introduction, Dc load line and Bias point.
Field effect Transistor: junction field effect transistor, JFET characteristics, MOSFET'S: Enhancement MOSFETs, Depletion Enhancement MOSFET's.

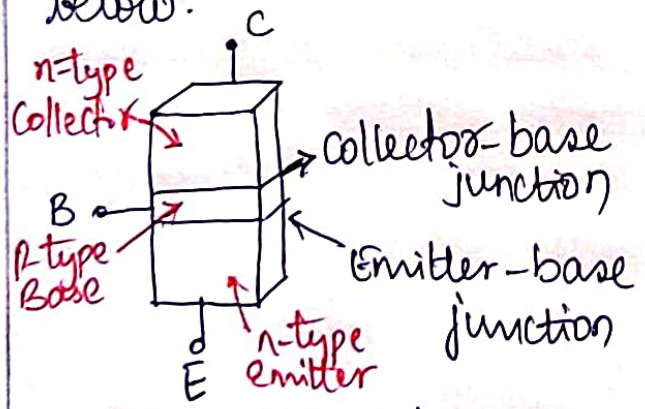
Introduction:

→ A bipolar junction transistor (BJT) has three layers of semiconductor material.

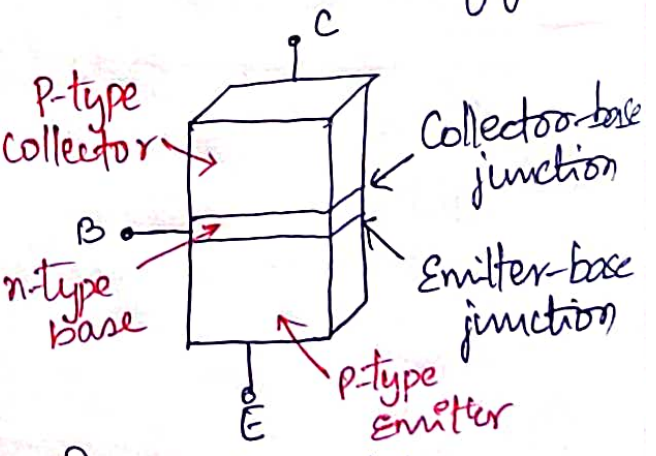
→ These are arranged either in npn sequence or in pnp sequence, and each of the three layers has a terminal.

→ The transistor can be used for current amplification

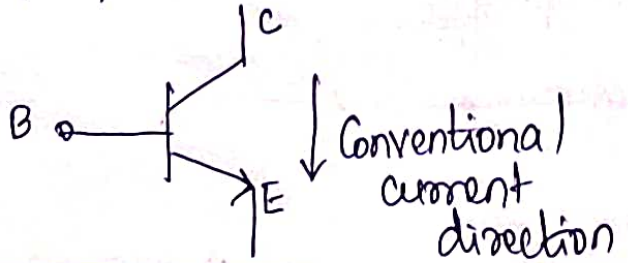
→ The two types of transistors are shown in figure below.

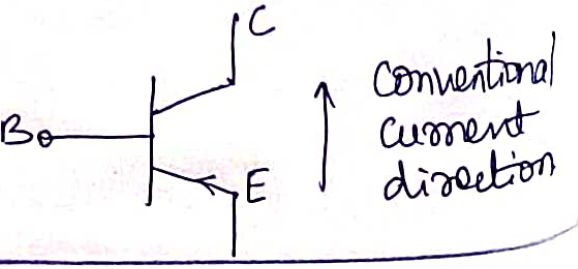


a) npn transistor



b) pnp transistor.

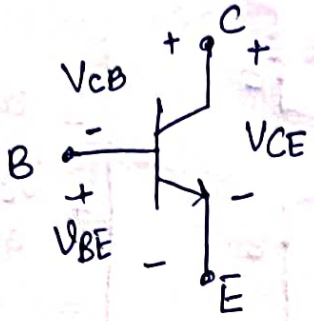




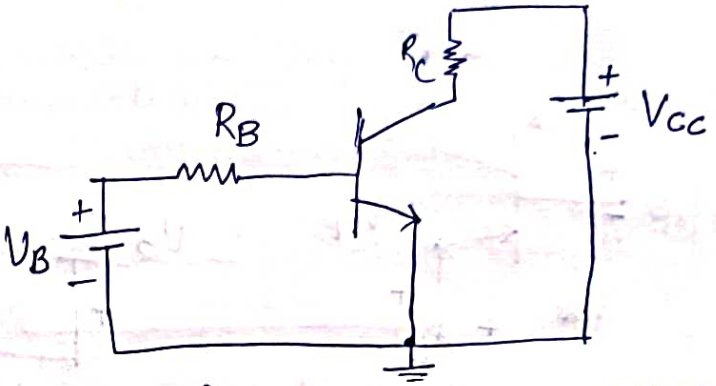
BJT Voltages and Currents:

Terminal Voltages: a) n-p-n transistor:

→ The terminal voltage polarities for an npn transistor are shown in figure below.



a) npn terminal voltage polarities



b) voltage source connection.

→ For an npn transistor, the base is biased positive w.r.t emitter, and collector is then biased to higher positive voltage than base.

→ Fig(b) shows, that the voltage sources are usually connected to the transistors via resistors.

→ The base voltage V_B is connected via resistor R_B, and the collector supply V_{CC} is connected via R_C.

→ The negative terminals of the two voltage sources are connected at the transistor emitter terminal.

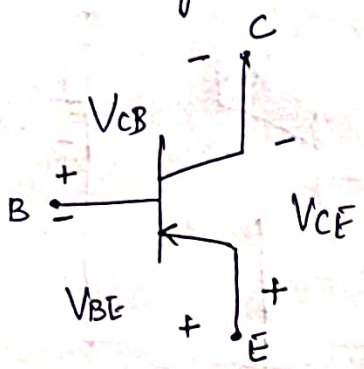
→ V_{CC} is always much larger than V_B and this ensures that the collector-base junction remains reverse-biased: positive on collector (n-side) and negative on base (p-side).

→ Typical transistor base-emitter voltages are similar to the diode forward voltages: 0.7V for a silicon transistor and 0.3V for a germanium device.

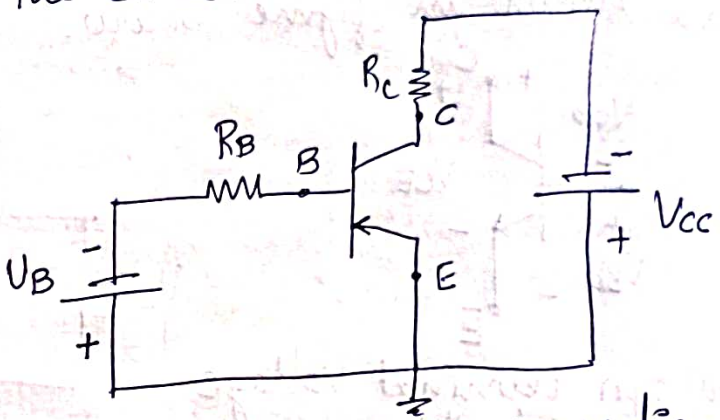
→ Collector voltages might be from 3V to 20V for many of a transistor.

b) pnp transistors:

→ For pnp device, the base is biased negative with respect to the emitter, and the collecter is made more negative than the base.



fig(a): pnp terminal Voltage polarities



b) voltage source connection.

→ Voltage sources are connected via resistor, and the source positive terminals connected at the emitter.

→ With V_{CC} larger than V_B, the collector is more negative than the (n-type) base and thus the collector-base junction is kept reverse-biased.

* All BJT's (npn & pnp) are normally operated with the collector-base junction reverse-biased and the base-emitter junction forward-biased.

Transistor Currents:

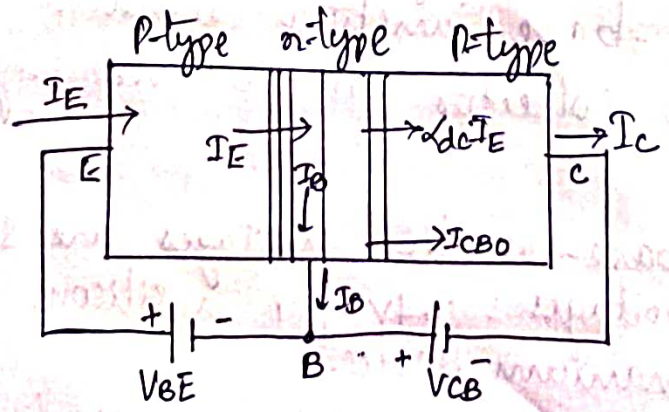
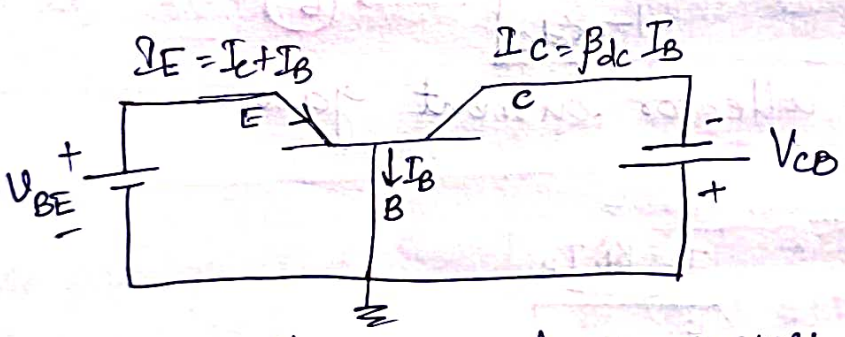


fig: Currents in a pnp transistors.

* The collector current (I_C) approximately equals to emitter current (I_E).
* The base current (I_B) is very much smaller than I_E.
* A very small reverse leakage current (I_{CBO}) occurs at the collector-base junction.
* The various current components that flow within a transistor is shown in figure.
* The current flowing into the emitter terminal is referred to as emitter current (I_E), collector terminal as collector current (I_C), base terminal as base current (I_B).
* Both I_C and I_B flow out of the transistor while I_E flows into the transistor.

$$\therefore \boxed{I_E = I_C + I_B} \longrightarrow (1).$$



* Most of the emitter current I_E crosses to the collector and only a small portion flows out of the base terminal.

$$\therefore \boxed{I_C = \alpha_{dc} \cdot I_E} \longrightarrow (2)$$

where, α_{dc} - emitter to collector current gain.

- Because the collector-base junction is reverse-biased, a very small reverse saturation current (I_{CBO}) flows across the junction.
- I_{CBO} is named as collector-base leakage current, and is normally small and it can be ignored.

Substitute Eqn (1) in (2),

$$I_C = \alpha_{dc}(I_C + I_B) \longrightarrow (3)$$

$$I_C = \alpha_{dc} I_C + \alpha_{dc} I_B.$$

$$I_C - \alpha_{dc} I_C = \alpha_{dc} I_B$$

$$I_C(1 - \alpha_{dc}) = \alpha_{dc} I_B$$

$$\boxed{I_C = \frac{\alpha_{dc} I_B}{1 - \alpha_{dc}}} \longrightarrow (4)$$

Eqn (4) can be written as,

$$\boxed{I_C = \beta_{dc} \cdot I_B} \longrightarrow (5)$$

where,

$$\boxed{\beta_{dc} = \frac{\alpha_{dc}}{1 - \alpha_{dc}}} \longrightarrow (6)$$

β_{dc} = base to collector current gain.

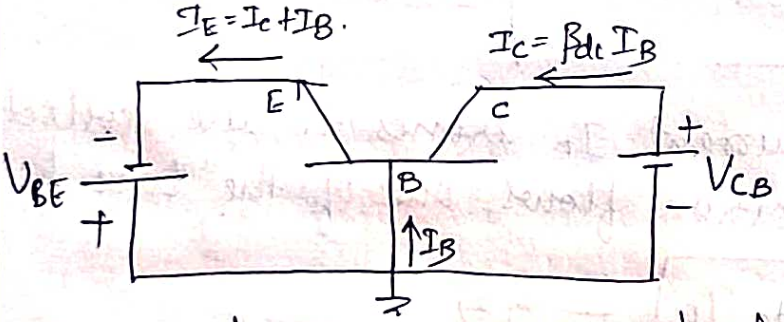


fig: Terminal currents for npn transistors.

* Here in npn transistor I_B and I_C are assumed to flow into the device and I_E is taken as flowing out.
* Since electrons are the majority charge carriers in npn transistor, they move in a direction opposite to conventional current direction.

problems:

① Calculate I_C and I_E for a transistor that has $\alpha_{dc} = 0.98$ and $I_B = 100\mu A$. Determine the value of β_{dc} for the transistor.

Soln: Given: $\alpha_{dc} = 0.98$, $I_B = 100\mu A$.

$\beta_{dc} = ?$ $I_C = ?$, $I_E = ?$

$$I_C = \frac{\alpha_{dc} I_B}{1-\alpha_{dc}} = \frac{0.98 \times 100\mu}{1-0.98}$$

$$\boxed{I_C = 4.9mA}$$

WKT, $I_C = \alpha_{dc} \cdot I_E$

$$I_E = \frac{I_C}{\alpha_{dc}} = \frac{4.9m}{0.98}$$

$$\boxed{I_E = 5mA}$$

WKT, $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.98}{1-0.98}$

$$\boxed{\beta_{dc} = 49}$$

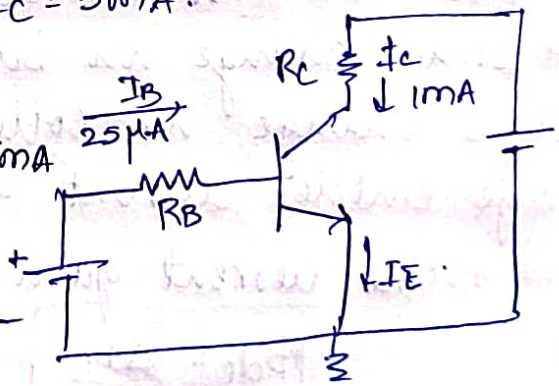
---

② Calculate α_{dc} and β_{dc} for the transistor shown, if I_C is measured as 1mA and I_B is 25μA. Determine the new base current to give $I_C = 5mA$.

Soln: Given: $\alpha_{dc} = ?$ $\beta_{dc} = ?$

$I_{Bnew} = ?$ for $I_C = 5mA$

$I_C = 1mA$ & $I_B = 25\mu A$



WKT, $\beta_{dc} = \frac{I_C}{I_B}$

$$= \frac{1mA}{25\mu}$$

$$\boxed{\beta = 40}$$

$I_E = I_C + I_B \Rightarrow I_E = 1mA + 25\mu A$, $\boxed{I_E = 1.025mA}$

WKT, $\alpha_{dc} = \frac{I_C}{I_E} = \frac{1mA}{1.025mA}$

$$\boxed{\alpha_{dc} = 0.976}$$

$$I_B = \frac{I_C}{\beta_{dc}} = \frac{5mA}{40}$$

$$\boxed{I_B = 125\mu A}$$

(3) Determine α_{dc} and I_B for a transistor that has I_C equal to 2.5mA and $I_E = 2.55mA$. Calculate β_{dc} for the transistor?

(4) A transistor has measured currents of $I_C = 3mA$ and $I_E = 3.03mA$. Calculate new current levels when the transistor is replaced with a device that has $\beta_{dc} = 75$. Assume that I_B remains constant.

BJT Amplification:

(1) Current Amplification:

WKT $I_C = \alpha_{dc} \cdot I_E \rightarrow (1)$

Thus, transistor can be used for current amplification.

* A small change in base current (ΔI_B) produces a large change in collector current (ΔI_C) and a large emitter current change (ΔI_E)

∴ The current gain from base to collector is

$$\boxed{\beta_{dc} = \frac{\Delta I_C}{\Delta I_B}} \longrightarrow (2)$$

* The increasing and decreasing levels of input and output currents may be defined as alternating quantities.

* The alternating current gain from base to collector is

$$\beta_{ac} = \frac{I_c}{I_b} \longrightarrow (3).$$

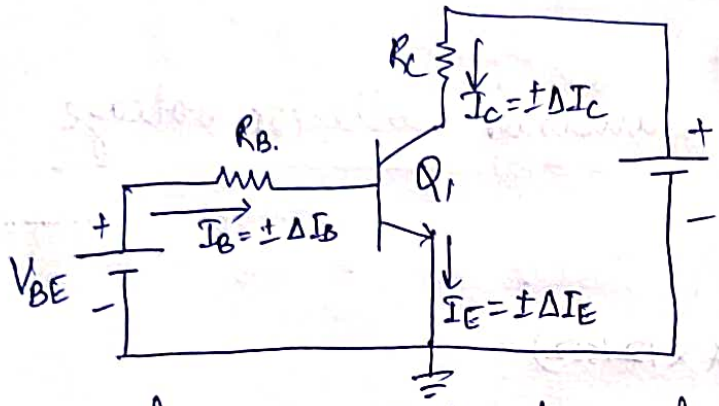
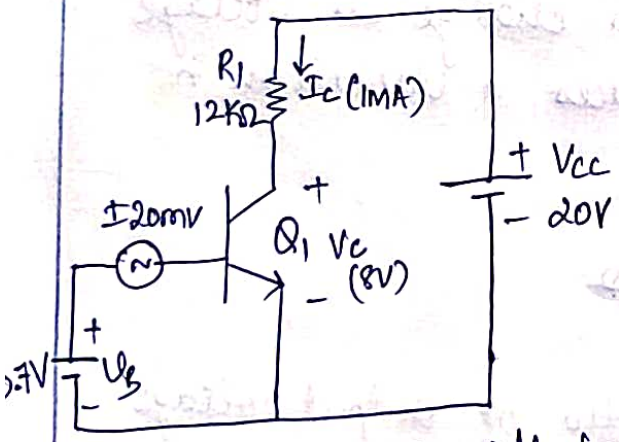


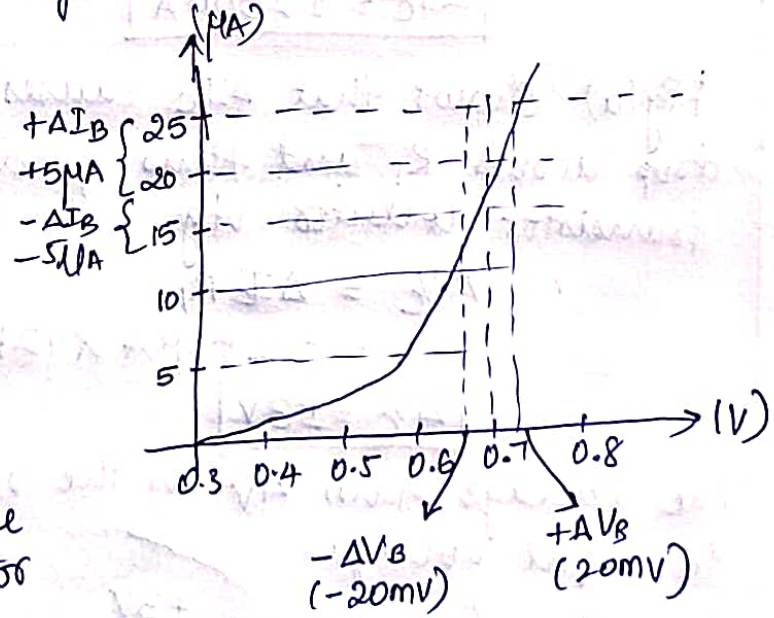
fig: current levels and current changes.

(2) Voltage Amplification:

→ Assume that the transistor Q_1 has $\beta_{dc} = 50$. The 0.7V dc voltage source (V_B) forward biases the transistor emitter-base junction.



a) Transistor circuit with base bias and signal generator



b) V_{BE} changes produce I_B changes

→ An ac signal source (V_i) in series with V_B provides a ±20mV input voltage.

→ The transistor collector is connected to a 20V dc voltage source V_{CC} via 12KΩ collector resistor R_1.

From fig (b) $I_B = 20\mu A$.

$\therefore I_C = \beta_{dc} \cdot I_B$

$= 50 \times 20\mu A$

$\boxed{I_C = 1mA}$

- The dc level of the transistor collector voltage can now be,

$V_C = V_{CC} - I_C R_L$

$= 20 - (1mA \times 12k\Omega)$

$\boxed{V_C = 8V}$

- The I_B change produces a change in collector current.

$\Delta I_C = \beta_{dc} \Delta I_B$

$= 50 \times (\pm 5\mu A)$

$\boxed{\Delta I_C = \pm 250\mu A}$

- Fig(a) shows that ΔI_C causes a change in voltage drop across R_1 and thus produces a variation in transistor collector Vtg.

$\Delta V_C = \Delta I R_1$

$= \pm 250\mu A \times 12k\Omega$

$\boxed{\Delta V_C = \pm 3V}$

- The voltage gain A_V is the ratio of output voltage to input voltage

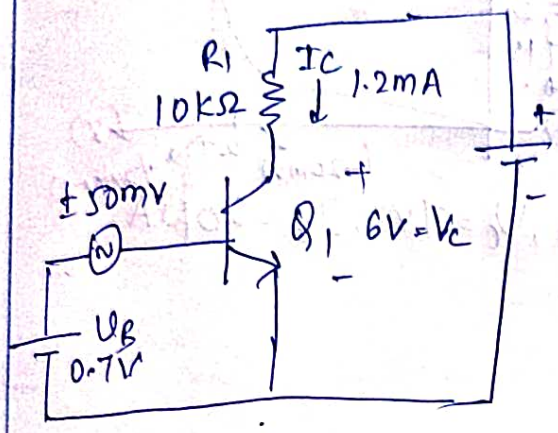
$A_C = \frac{\Delta V_C}{\Delta V_B} = \frac{\pm 3V}{\pm 20mV}$

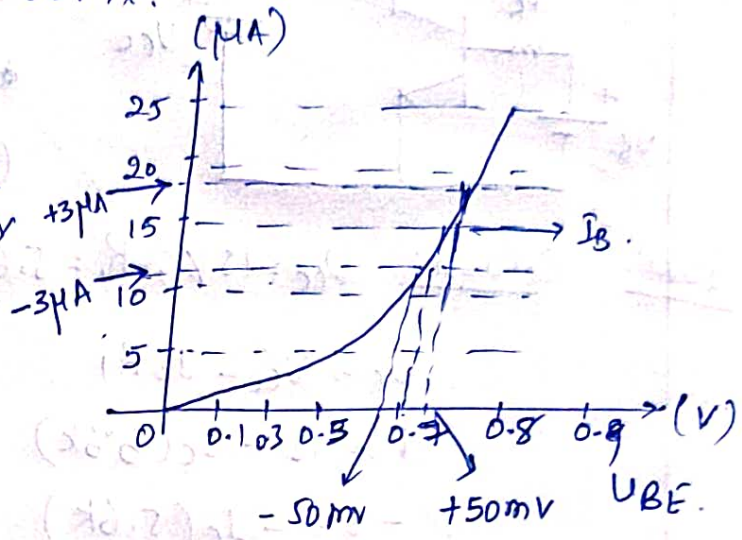
$\boxed{A_V = 150}$

$\therefore$ The circuit ac input is the base voltage change ΔV_B and the ac output is the collector voltage change (ΔV_C). Because the output is greater than the input, the circuit has a voltage gain. It is a voltage amplifier.

Problem.

(1) Determine the dc collector voltage for the circuit (a) below. If the transistor has the I_B/V_{BE} characteristics shown in fig (b) and $\beta_{dc} = \beta_{ac} = 80$. Calculate the circuit voltage gain when $V_i = \pm 50mV$.





Soln: Given.

$I_B = 15\mu A$. for $V_B = 0.7V$

$I_C = \beta_{dc} \cdot I_B = 80 \times 15\mu A$

$\boxed{I_C = 1.2mA}$

$V_C = V_{CC} - I_C R_1$

$= 18 - (1.2m \times 10K)$

$\boxed{V_C = \pm 6V}$

from fig, $I_b = \pm 3\mu A$, for $V_i = \pm 50mV$.

$I_c = \beta_{ac} I_b$

$= 80 \times \pm 3\mu A$

$\boxed{I_c = \pm 240\mu A}$

$V_o = I_c R_1 = \pm 240\mu A \times 10K\Omega$

$\boxed{V_o = \pm 2.4V}$

$A_V = \frac{V_o}{V_i} = \frac{\pm 2.4V}{\pm 50mV} = 48.$

$\boxed{A_V = 48}$

BJT Biasing - process of setting or providing DC voltage which helps in the functioning of the circuit.

DC Load LINE & BIAS POINT :-

DC Load Line :-

* The DC load line for a transistor circuit is a straight line drawn on the transistor o/p characteristics.
* For common emitter (CE) circuit, the load line is a graph of collector current (I_C) versus collector-emitter voltage (V_{CE}). for a given value of collector resistance (R_C) & a given supply voltage (V_{CC}).
* The load line shows all corresponding levels of I_C & V_{CE} that can exist in a particular circuit.

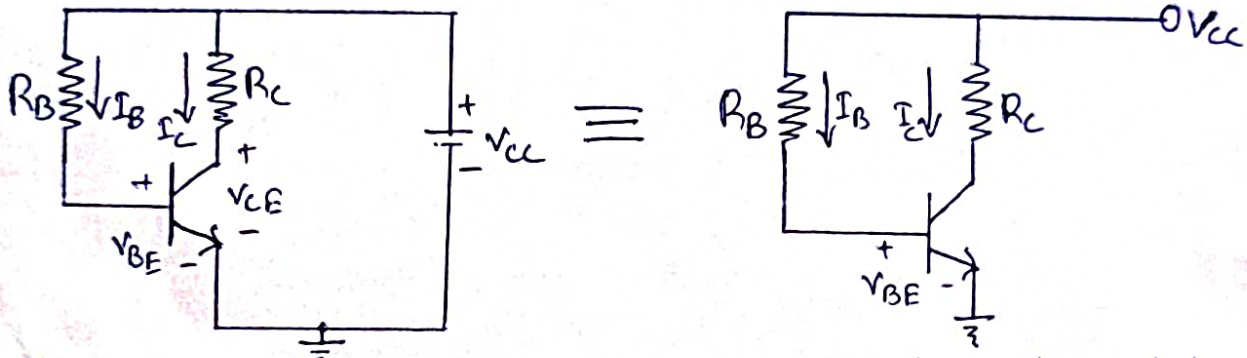


fig ① Transistor in CE configuration biased in Active region

* consider an NPN transistor in CE configuration biased in active region.
* The dc supply voltage V_{CC} forward biases the base-emitter junction & reverse biases the collector-base junction.

Applying KVL to collector-emitter ckt we have,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$I_C R_C = V_{CC} - V_{CE} \longrightarrow ①$$

$$I_C = \frac{V_{CC}}{R_C} - \frac{V_{CE}}{R_C} \quad \text{or} \quad \boxed{I_C = \frac{V_{CC} - V_{CE}}{R_C}}$$

$$\boxed{I_C = V_{CE}\left(-\frac{1}{R_C}\right) + \frac{V_{CC}}{R_C}} \rightarrow ② \quad \text{OR.} \quad \boxed{I_C = \left[-\frac{1}{R_C}\right] V_{CE} + \frac{V_{CC}}{R_C}} \rightarrow ②$$

* Equation ② is similar to the equation representing a straight line i.e $\boxed{y = mx + c}$

$$I_c = \left(-\frac{1}{R_c}\right) V_{CE} + \frac{V_{cc}}{R_c}$$
$$y = mx + c$$

{ By comparison it is noted that along y-axis we have I_c & along x-axis we have V_{CE} with slope of line $m = -1/R_c$ }.

* To obtain a straight line consider 2 different conditions

1) put $I_c = 0$, in eq ①

2) put $V_{CE} = 0$, in eq ②

i.e. $I_c R_c = V_{cc} - V_{CE} \rightarrow ①$

1) When $I_c = 0$, then $V_{CE} = V_{cc}$

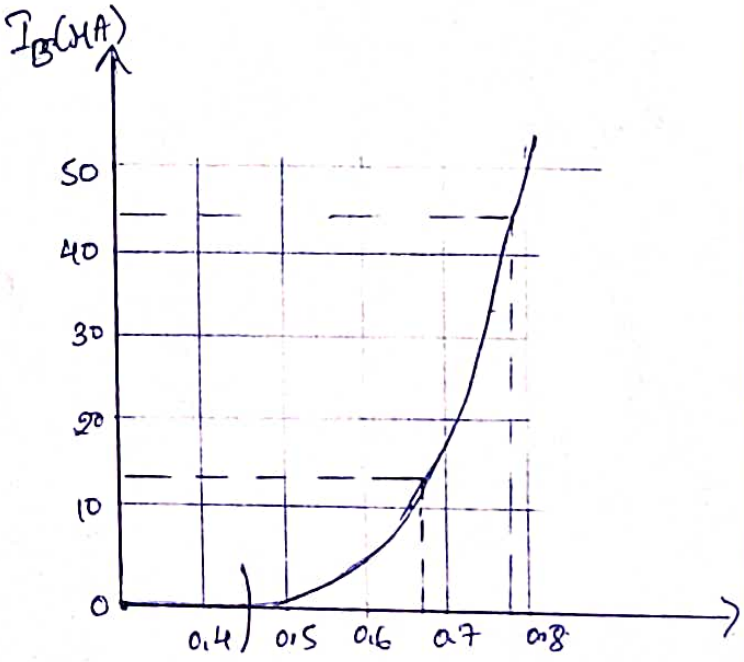
i.e. $0 = V_{cc} - V_{CE}$.

$$\boxed{V_{CE} = V_{cc}} \rightarrow ③$$

2) When $V_{CE} = 0$, then $I_c = \frac{V_{cc}}{R_c}$

i.e. $I_c R_c = V_{cc} - 0$.

$$\boxed{I_c = \frac{V_{cc}}{R_c}} \rightarrow ④.$$



b) Input characteristic of transistor.

* From eq ③ & ④ we will obtain a straight line on the o/p characteristics curve of the transistor circuit with 2 extreme points being $(V_{CE}, I_c) = (V_{cc} - V_{cc}/R_c)$.

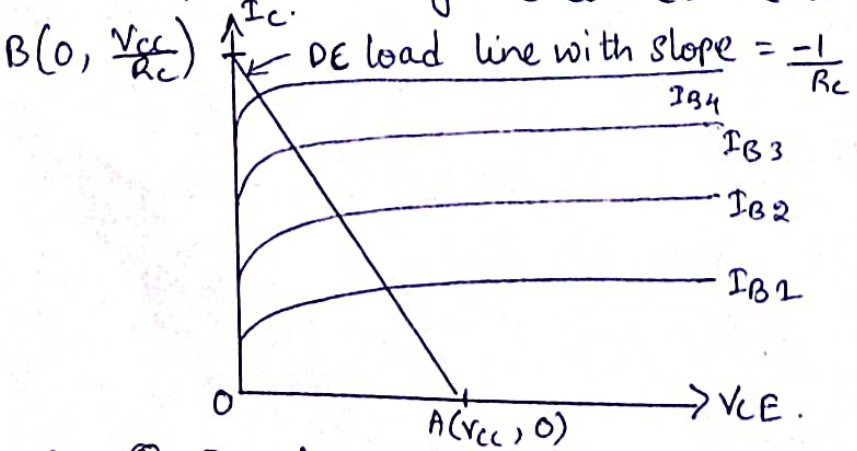
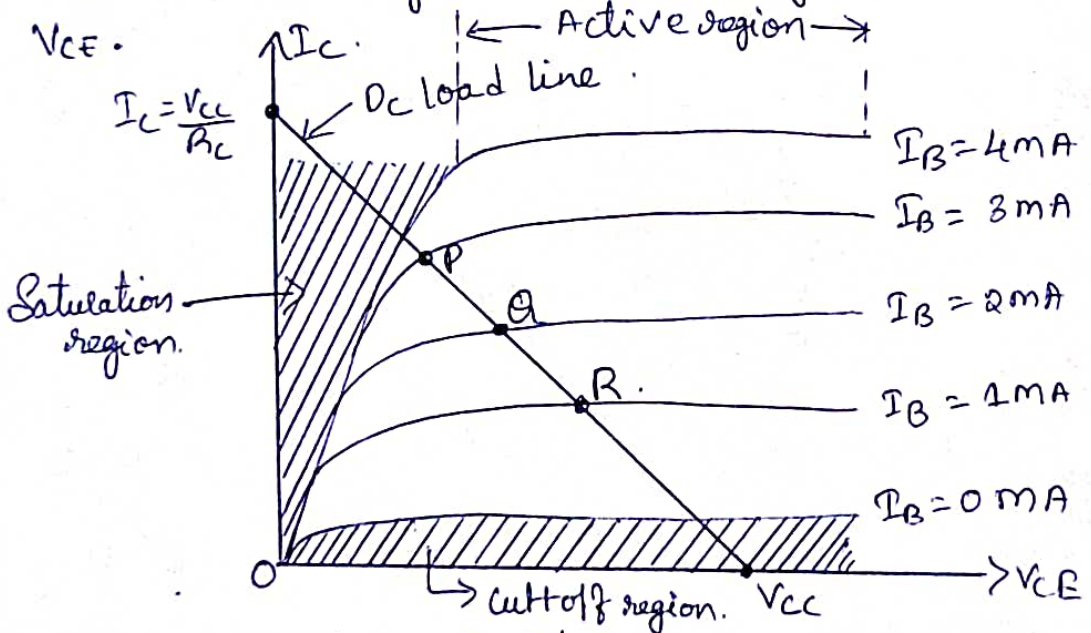


fig ② DC load line drawn on transistor CE o/p characteristics.

* The straight line obtained by joining (V_{CE}, I_C) these points is called the DC load line as shown in above figure.

DC Bias point or Q-point or dc operating point or Quiescent point :-

* Q-point identifies the transistor collector current (I_C) and collector-emitter voltage (V_{CE}) when there is no I/p signal at the base terminal.
* the intersection of DC load line with the o/p characteristic curve gives the co-ordinates of the Q-point.
* When a signal is applied to the transistor base, I_B varies according to the instantaneous amplitude of the signal. This causes I_C to vary & consequently produces a variation in V_{CE}.



Effect of Emitter Resistor :-

* In fig (a) resistor R_E is in series with the transistor emitter terminal & the supply voltage connected directly to the collector terminal.
* R_E is the dc load.

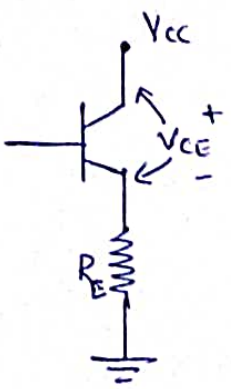


fig (a) $R_L(dc) = R_E$

* By applying KVL to collector-emitter ckt

$$V_{CC} - V_{CE} - I_E R_E = 0 \rightarrow (1)$$

assuming $\boxed{I_E \approx I_C}$

$$V_{CC} - V_{CE} - I_C R_E = 0.$$

$$I_C R_E = V_{CC} - V_{CE} \rightarrow (2)$$

$$I_C = \frac{V_{CC} - V_{CE}}{R_E}.$$

$$I_C = -\frac{V_{CE}}{R_E} + \frac{V_{CC}}{R_E}.$$

$$\boxed{I_C = \left(\frac{-1}{R_E}\right) V_{CE} + \frac{V_{CE}}{R_E}} \rightarrow (3)$$

i) put $I_C = 0$ in eq (2).

$$\boxed{V_{CE} = V_{CC}} \rightarrow (4)$$

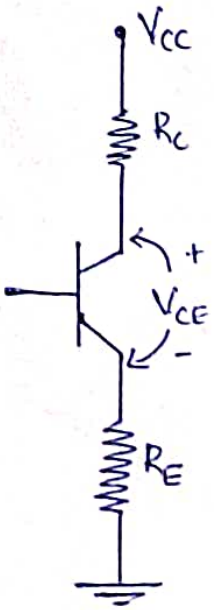
(ii) put $V_{CE} = 0$ in eq (2)

$$\boxed{I_C = \frac{V_{CC}}{R_E}} \rightarrow (5)$$

eq (4) & (5) are the dc load lines point.

(ii) <u>With R_E & R_C :-</u>

* In fig (b), both collector & emitter resistor R_C & R_E are present, & the total dc load in series with the transistor is $(R_C + R_E)$.



* Assuming $I_E \approx I_C$.

* Applying KVL to collector emitter circuit,

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0.$$

$\boxed{I_E \approx I_C}$

$$V_{CC} - I_C R_C - V_{CE} - I_C R_E = 0.$$

$$V_{CC} - I_C [R_C + R_E] - V_{CE} = 0.$$

$$I_C [R_C + R_E] = V_{CC} - V_{CE} \longrightarrow (2)$$

$$I_C = \frac{V_{CC} - V_{CE}}{[R_C + R_E]}$$

$$I_C = -\frac{V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E}$$

$$\boxed{I_C = \left[-\frac{1}{R_C + R_E}\right] V_{CE} + \frac{V_{CC}}{R_C + R_E}} \longrightarrow (3)$$

i) put $I_C = 0$ in eq (2)

$$\boxed{V_{CE} = V_{CC}} \longrightarrow (4)$$

ii) put $V_{CE} = 0$ in eq (2).

$$\boxed{I_C = \frac{V_{CC}}{R_C + R_E}} \longrightarrow (5)$$

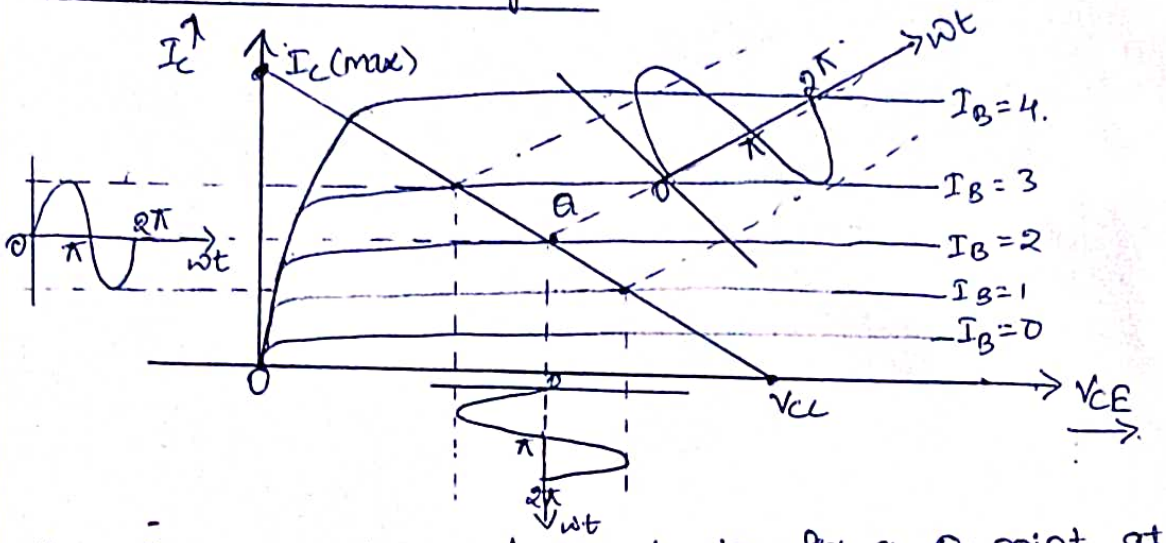
eq (4) & (5) are the dc load lines point.

Selection of operating point :-

* The operating point can be selected at three different positions on the dc load line ie.

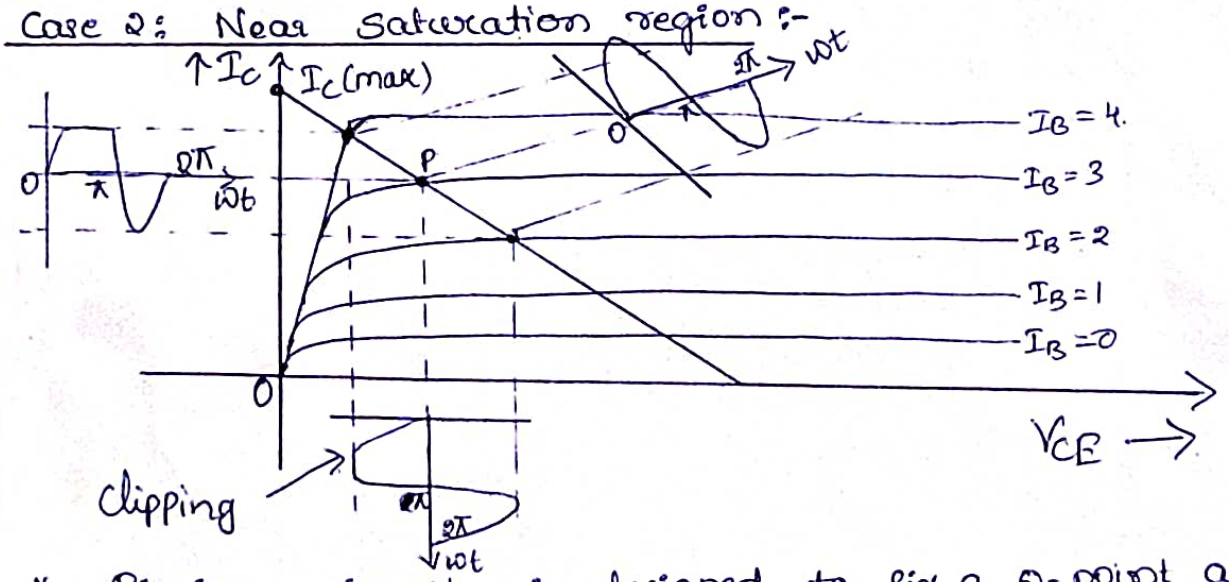
1) In Active region.
2) Near Saturation region.
3) Near cut-off region.

Case 1 : In Active region :-



* Biasing ckt is designed to fix a Q-point at point 'Q' as shown in fig. i.e at the centre of active region. The o/p signal is sinusoidal waveform without any distortion. Thus point Q is the best operating point.

Case 2 : Near Saturation region :-

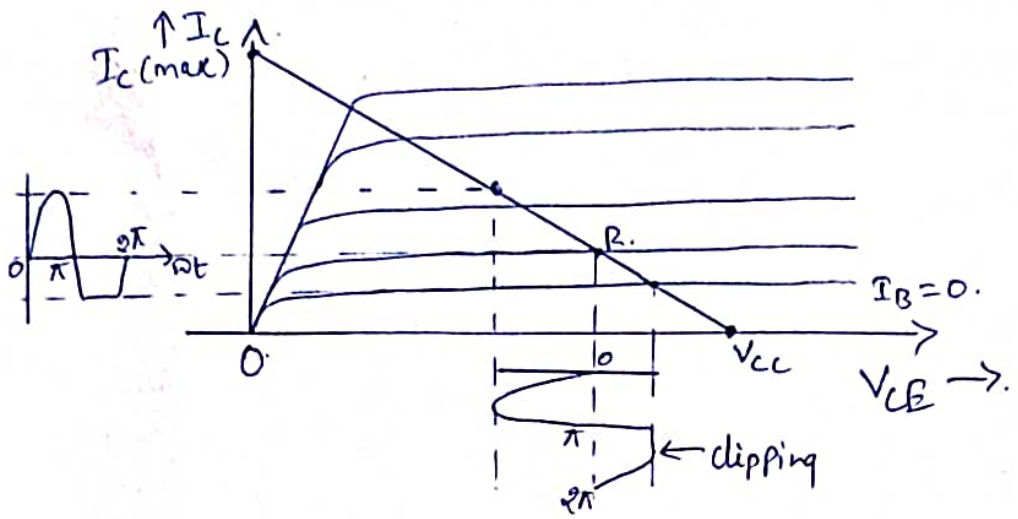


* Biasing ciacuit is designed to fix a Q-point at point 'p' as shown in above figure. point 'p' is very near to the Saturation region.

* The o/p signal is clipped at the positive half cycle i.e. distortion is present at the o/p.

∴ point 'p' is not a suitable operating point.

Case 3 : Near cut-off region :-



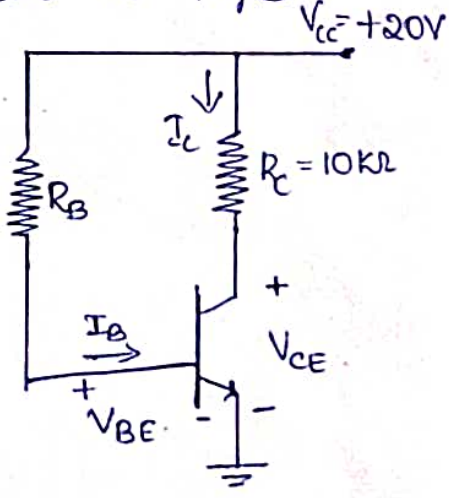
* Biasing circuit is designed to fix a Q-point at point 'R' as shown in above figure. point 'R' is very near to the cut-off region.

* The o/p signal is clipped at the negative half cycle i.e distortion is present at the o/p.

∴ point 'R' is not a suitable operating point.

---

1) Draw the dc load line for the circuit in fig ①



Apply KVL to collector emitter ckt

$$V_{CC} - I_C R_C - V_{CE} = 0.$$

$$\boxed{V_{CE} = V_{CC} - I_C R_C} \longrightarrow ①$$

1) To find V_{CE}, put $I_C = 0$ in eq ①

$$V_{CE} = V_{CC} - 0.$$

$$\boxed{V_{CE} = 20\,V}$$

2) To find I_C, put $V_{CE} = 0$ in eq ①

$$0 = 20V - I_C\,(10K\Omega)$$

$$I_C\,(10K\Omega) = 20V$$

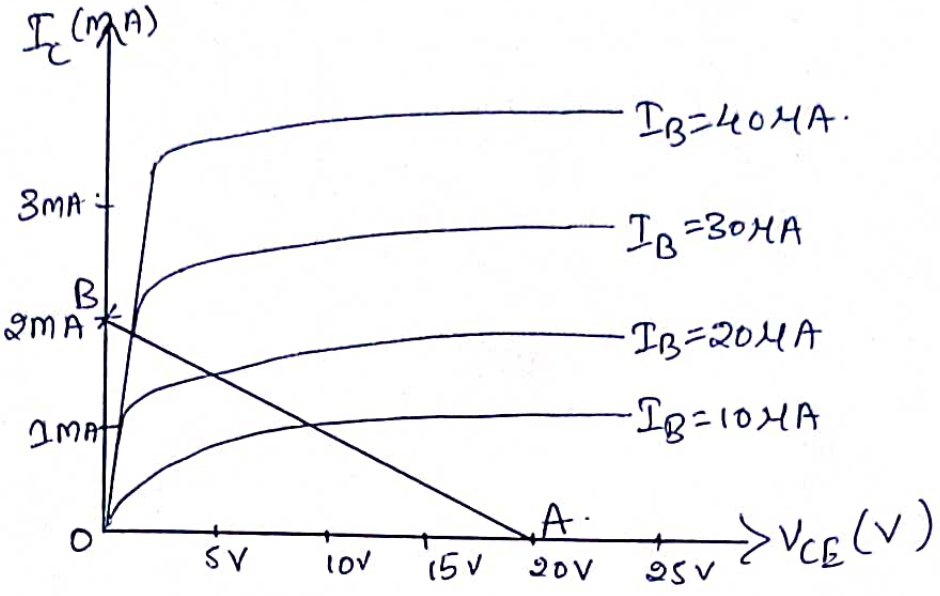
i.e $V_{CE} = V_C - I_C R_C$

$$0 = V_{CC} - I_C R_C$$

$$I_C R_C = V_{CC}$$

$$I_C = V_{CC} / R_C$$

$$I_c = \frac{20V}{10K\Omega} = 2mA.$$



DC Load line points :

1) $I_C = 0$, $V_{CE} = 20V$	i.e Point A
2) $V_{CE} = 0$, $I_c = 2mA$	i.e Point B.

---

2. Draw the new dc load line for the circuit in fig ① when $R_c = 12\,K\Omega$

WKT. $V_{CE} = V_{cc} - I_c R_c$ —①

(1) put $I_c = 0$ in eq ①.

$V_{CE} = V_{cc}$.

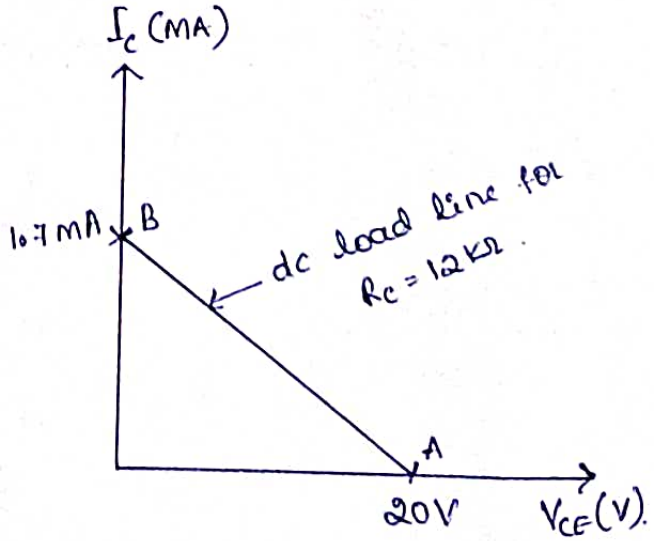
$\boxed{V_{CE} = 20V}$

(2) put $V_{CE} = 0$ in eq ①.

$0 = V_{cc} - I_c R_c$

$I_c = \frac{V_{cc}}{R_c} = \frac{20V}{12K\Omega}$

$\boxed{I_c = 1.7\ mA}$



3) The transistor ckt in fig ① has the collector characteristics as shown in fig ②. Determine the circuit Q-point & estimate the maximum symmetrical o/p voltage swing. Note that $V_{CC} = 18\ V$, $R_C = 2.2\ k\Omega$ & $I_B = 40\ \mu A$.

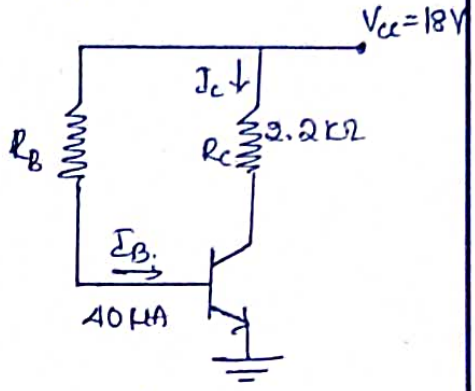


fig ①.

Sol:

Dc load line:-

WKT $V_{CE} = V_{cc} - I_c R_c$ — ①

1) put $I_c = 0$ in eq ①

$V_{CE} = V_{CC}$.

$\boxed{V_{CE} = 18\ V}$ point A.

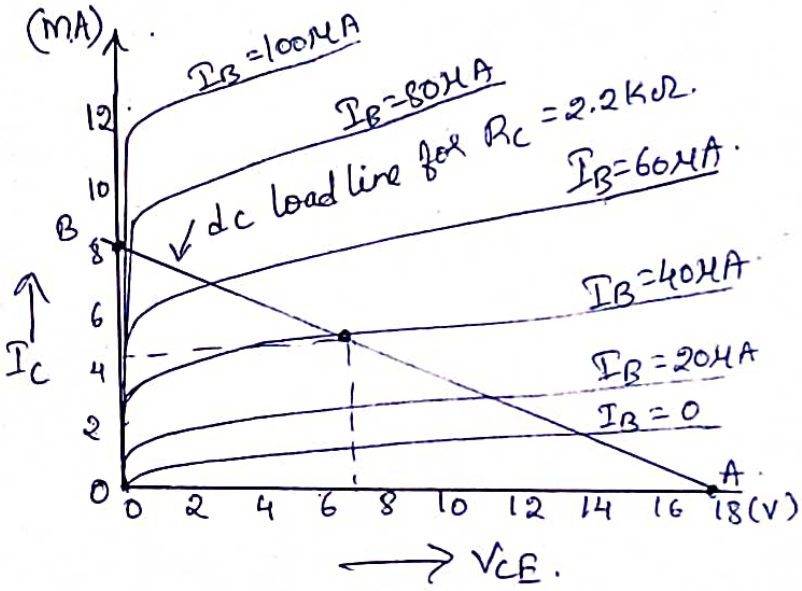
2) put $V_{CE} = 0$ in eq ①

$V_{CE} = V_{cc} - I_c R_c$

$0 = V_{cc} - I_c R_c$

$I_c = \frac{V_{CC}}{R_c} = \frac{18\ V}{2.2\ k\Omega}$

$\boxed{I_c = 8.2\ mA}$ point B.



* Draw the dc load line through points A & B. The Q-point is at the intersection of the load line & the $I_B = 40\ \mu A$ characteristics.

* the dc Bias conditions are

$\boxed{I_c \approx 4.1\ mA \text{ \& } V_{CE} \approx 9V}$

* The maximum symmetrical o/p voltage swing is

$\boxed{\Delta V_{CE} \approx +9V}$

* Calculate α_{dc} and β_{dc} for the transistor if I_c is measured as 1mA and I_B is 25μA. Also determine the new base current to give $I_c = 5mA$.

June-08, 6M

Given:- (i) $I_c = 1mA$, $I_B = 25\mu A$, $\alpha_{dc} = ?$ $\beta_{dc} = ?$

(ii) $I_c = 5mA$, $I_B = ?$

Sol:-

i) * $\beta_{dc} = \frac{I_c}{I_B} = \frac{1mA}{25\mu A} = 40.$

* $\alpha_{dc} = \frac{\beta_{dc}}{1+\beta_{dc}} = \frac{40}{1+40} = 0.9756.$

ii) When $I_c = 5mA$

* $I_B = \frac{I_c}{\beta_{dc}} = \frac{5mA}{40} = 125\mu A.$

---

* Calculate the values of I_c, I_E and β_{dc} for a transistor with $\alpha_{dc} = 0.98$ and $I_B = 120\mu A$.

Jan-09, 4M

Given: $\alpha_{dc} = 0.98$, $I_B = 120\mu A$, $I_c = ?$, $I_E = ?$ & $\beta_{dc} = ?$

Sol:

* $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}} = \frac{0.98}{1-0.98} = \underline{\underline{49}}$

* $I_c = \beta_{dc} I_B = 49 \times 120\mu A = 5.88mA.$

---

* Given $I_E = 2.5mA$, $\alpha = 0.98$ and $I_{CBO} = 10\mu A$, Calculate I_B and I_c

Jan-11, 4M

Sol:- WKT $\alpha = \frac{I_c}{I_E}$

$I_c = \alpha I_E = 0.98 \times 2.5mA$

$I_c = 2.45mA$

NKT $I_E = I_B + I_C$

$I_B = I_E - I_C = 2.5\,mA - 2.45\,mA$

$\boxed{I_B = 50\,\mu A}$

---

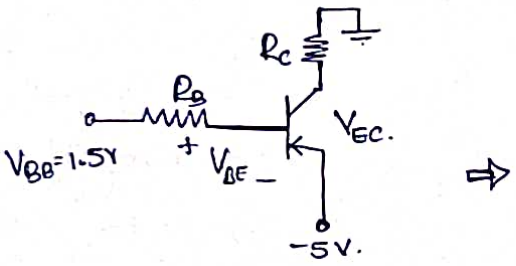
* For the circuit shown below, the parameters are $V_{BB} = 1.5V$, $R_B = 580\,K\Omega$, $V_{CC} = 5V$, $V_{EB(ON)} = 0.6V$ and $\beta = 100$. Find I_B, I_C, I_E and R_C such that $V_{EC} = 1/2(V_{CC})$.

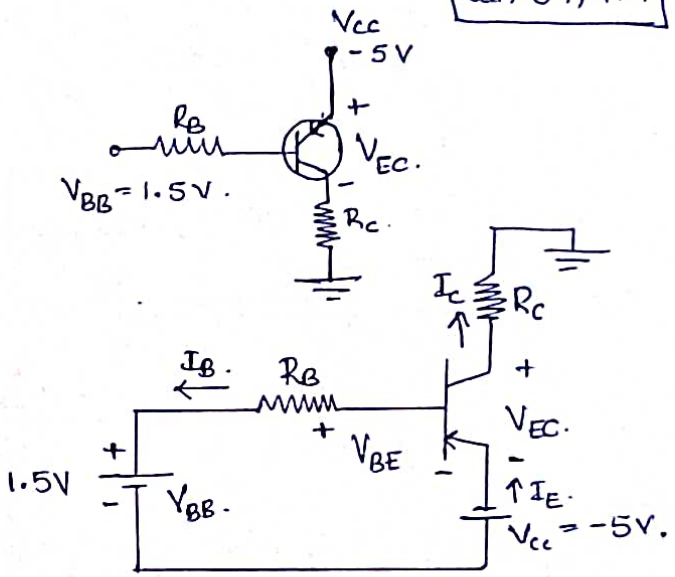
Jan-07, 7M

Given :-

$V_{EC} = 2.5V$.

Sol:-





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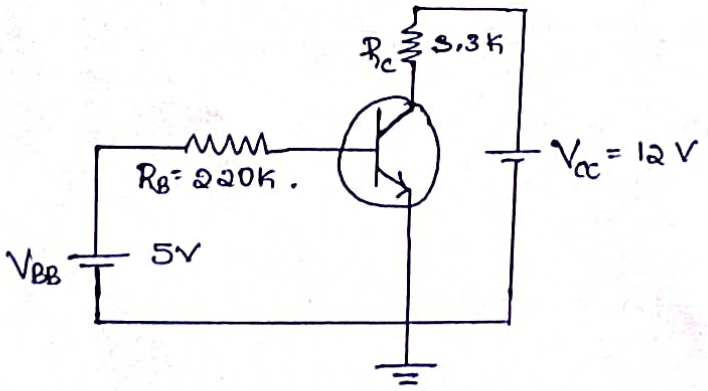
* Determine the transistor currents in the fig if $\beta = 100$.

June-09, 8M



Given:- $V_{CC} = 12V$, $V_{BB} = 5V$, $R_B = 220K\Omega$, $R_C = 3.3K\Omega$ & $\beta = 100$ assuming $V_{BE} = 0.7V$.

Sol:-

Applying KVL to the I/p ckt.

$$V_{BB} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{5V - 0.7V}{220K\Omega}$$

$$\boxed{I_B = 19.545\,\mu A}$$

$$I_C = \beta I_B = 100 \times 19.545\,\mu A$$

$$\boxed{I_C = 1.954\,mA}$$

$$I_E = I_B + I_C = 19.545\,\mu A + 1.954\,mA$$

$$\boxed{I_E = 1.974\,mA}$$

Applying KVL from V_{CC}, V_{BE} & V_{BB}.

$$-V_{CC} + V_{BE} - I_B R_B - V_{BB} = 0$$

$$-V_{CC} - V_{BB} + V_{BE} = I_B R_B.$$

$$I_B = \frac{-V_{CC} - V_{BB} + V_{BE}}{R_B} = \frac{-5V - 1.5V + 0.6V}{580K\Omega} = \frac{-5.9V}{580K\Omega}$$

* $\boxed{I_B = -10.17\,\mu A}$

* $I_C = \beta I_B = 100 \times 10.17\,\mu A$

$$\boxed{I_C = 1.017\,mA}$$

* $I_E = I_B + I_C = 10.17\,\mu A + 1.017\,mA$

$$\boxed{I_E = 1.027\,mA}$$

* Applying KVL from V_{CC}, V_{EB} & R_c.

$$-V_{CC} + V_{EB} - I_c R_c = 0.$$

$$I_c R_c = -V_{CC} + V_{EB}$$

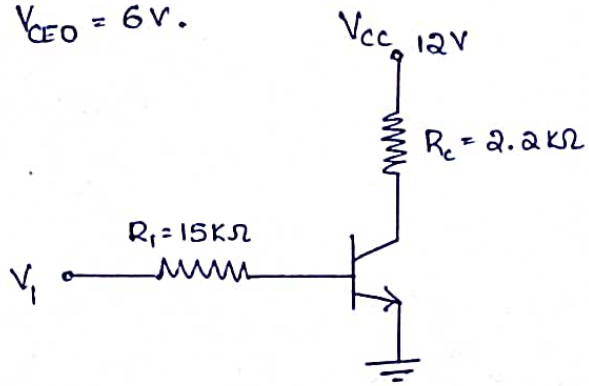
$$R_c = \frac{-V_{CC} + V_{EB}}{I_c} = \frac{-5V + 2.5V}{1.027\,mA}$$

$$\boxed{R_c = 2.43\,K\Omega}$$

---

* For the transistor in fig $\beta = 30$, determine V_1 such that $V_{CEQ} = 6V$.

June-07, 5M



Given :- $V_{CC} = 12V$, $R_1 = 15\,K\Omega$, $R_c = 2.2\,K\Omega$, $V_{CE} = 6V$, $\beta = 30$.

Sol:- Applying KVL to o/p ckt

$$V_{CC} - I_c R_c - V_{CE} = 0$$

$$I_c R_c = V_{CC} - V_{CE}$$

$$I_c = \frac{V_{CC} - V_{CE}}{R_c} = \frac{12V - 6V}{2.2K\Omega}$$

* $\boxed{I_c = 2.72\,mA}$

* $$I_B = \frac{I_c}{\beta} = \frac{2.72\,mA}{30}.$$

$$\boxed{I_B = 90.90\,\mu A}$$

Applying KVL to I/p Ckt.

$$V_1 - I_B R_B - V_{BE} = 0$$

$$V_1 = I_B R_B + V_{BE} = (90.90\,\mu A \times 15\,K\Omega) + 0.7\,V.$$

$$\boxed{V_1 = 2.06\ V}$$

---

1) calculate I_c & I_E for a transistor that has $\alpha_{dc} = 0.98$ & $I_B = 100\,\mu A$. Also determine the value of β_{dc} for the transistor. (Reference book).

Sol:

* $I_c = \dfrac{\alpha_{dc}}{1-\alpha_{dc}} I_B = \dfrac{0.98}{1-0.98} \times 100\,\mu A = 4.9\,mA$

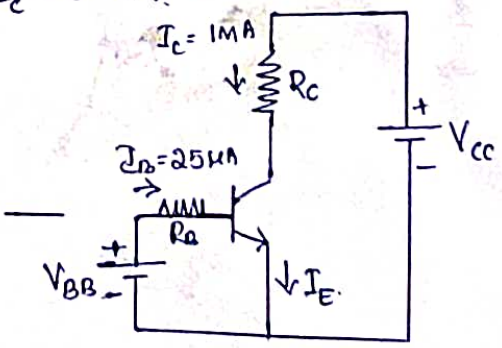
* $I_c = \alpha_{dc} I_E$,

$$I_E = \frac{I_c}{\alpha_{dc}} = \frac{4.9\,mA}{0.98} = 5\,mA$$

* $\beta_{dc} = \dfrac{\alpha_{dc}}{1-\alpha_{dc}} = \dfrac{0.98}{1-0.98} = 49.$

---

2) Calculate α_{dc} & β_{dc} for the transistor in fig ① If I_c is measured as 1mA, & I_B is 25 μA. Also determine the new base current to give $I_c = 5mA$.



(Reference book)

Sol:

* $\beta_{dc} = \dfrac{I_c}{I_B} = \dfrac{1mA}{25\,\mu A} = 40$

* $I_E = I_B + I_c = 1mA + 25\,\mu A$
$= 1.025\,mA$

* $\alpha_{dc} = \dfrac{I_c}{I_E} = \dfrac{1mA}{1.025\,mA} = 0.976$

* New base current to give $I_c = 5mA$

$I_B = I_c / \beta_{dc} = 5mA/40 = 125\,\mu A.$

δ) A transistor has $I_B = 100\,\mu A$ & $I_c = 2mA$, find

July 06, 10 M

i) β of the transistor.

ii) α of the transistor.

iii) emitter current I_E

iv) If I_B changes by $+25\,\mu A$ & I_c changes by $+0.6\,mA$. find the new value of β.

Sol:- Given : $I_B = 100\,\mu A$ & $I_c = 2mA$;

i) $\beta = \frac{I_c}{I_B} = \frac{2mA}{100\,\mu A} = 20$

ii) $\alpha = \frac{\beta}{1+\beta} = \frac{20}{1+20} = 0.952$.

iii) $I_E = I_B + I_c = 100\,\mu A + 2mA = 2.1\,mA$

iv) New $I_B = 100\,\mu A + 25\,\mu A = 125\,\mu A$

New $I_c = 2mA + 0.6\,mA = 2.6\,mA$

New $\beta = \frac{2.6mA}{125\,\mu A} = 20.8$

---

4. If α for a transistor is 0.99, the base current is $100\,\mu A$, estimate the collector current.

March - 99, 5M

Sol: Given $I_B = 100\,\mu A$, $\alpha = 0.99$

WKT. $\beta = \frac{I_c}{I_B}$ & $\beta = \frac{\alpha}{1-\alpha}$

$\beta = \frac{0.99}{1-0.99} = \underline{\underline{99}}$

$I_c = \beta I_B$

$= 99 \times 100\,\mu A$

$I_c = 9.9\,mA$

* $A_V = \frac{V_o}{V_i} = \frac{\pm 5.1\ V}{\pm 50\ mV} = 102.$

* The decrease in R_c reduces the voltage gain.

(c) With change in transistor $V_c = 9V$, for $V_{BE} = 0.7V$

$I_B = 30\ \mu A$.

$$\boxed{V_o = V_{RC} = I_C R_C}$$

$\therefore$ WKT. $V_c = V_{cc} - I_C R_C$

$I_C R_C = V_{cc} - V_c$.

$= 25V - 9V$

$$\boxed{I_C R_C = 16\ V}$$

$$I_C = \frac{16\ V}{12\ K\Omega} = 1.33\ mA$$

* $\beta_{dc} = \frac{I_c}{I_B} = \frac{1.33\ mA}{30\ \mu A}$

$$\boxed{\beta_{dc} = 44.33}$$

Input - Output Characteristics of CB, CE & CC Configurations.

Common Base Characteristics :- (NPN).

* Draw input and output characteristics of a transistor in common base configuration and explain in detail.

Jan 09, 8M

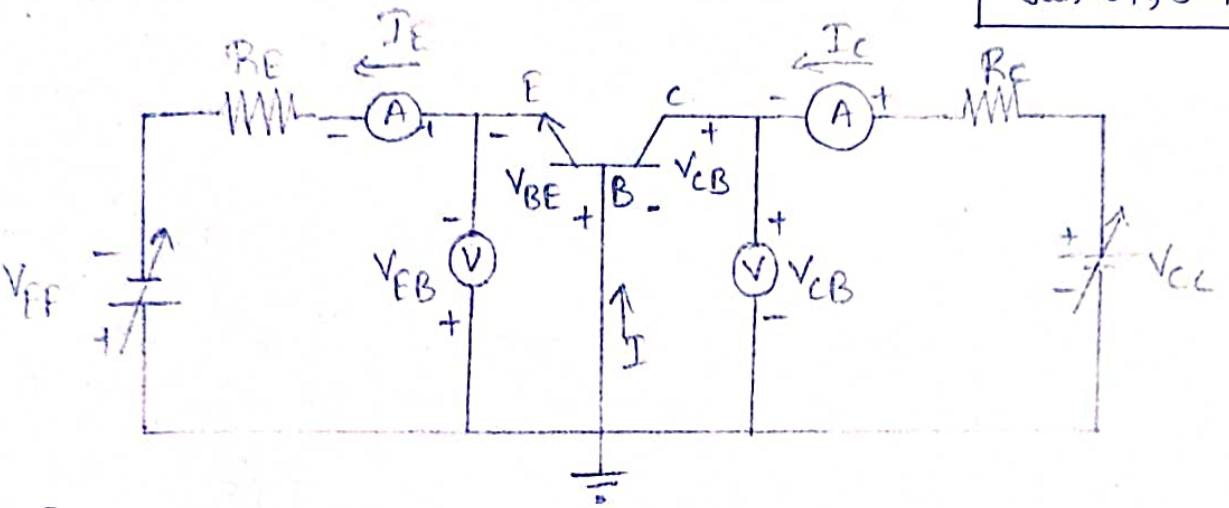


fig ① Common base configuration.

{ * In fig ①, the emitter - base Junction (JE) is forward biased & the collector - base Junction (JC) is reverse biased.

* The emitter current I_E flows in the I/p ckt & the collector current I_C flows in the o/p ckt.

}.

I/p Characteristics :-

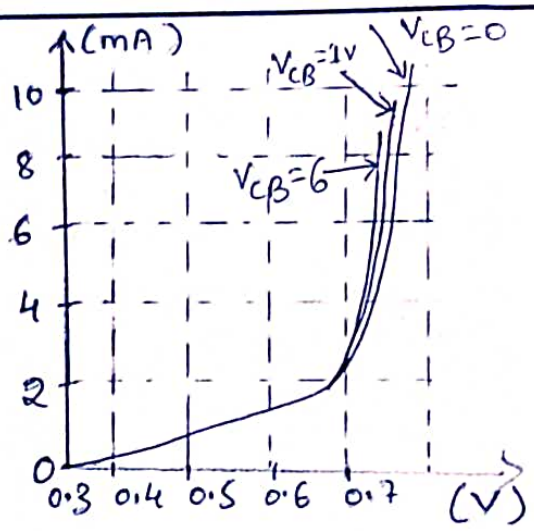
* It is the curve between emitter current 'I_E' & emitter to base voltage 'V_{EB}' at constant collector - base voltage 'V_{CB}'.

* The emitter current is generally taken along Y-axis & emitter base voltage along x-axis as shown in fig ②.

{ 1) Keep o/p voltage V_{CB} to constant.

2) Increase I/p voltage V_{EB} in small suitable steps.

3) Note down the corresponding I/p current 'I_E'.



* To obtain the I/p characteristics, the o/p voltage 'V_{CB}' is kept constant, I/p voltage 'V_{EB}' is varied in small intervals & the corresponding change in I/p current 'I_E' is recorded.

* I_E is then plotted against V_{EB} as shown in fig ③. The experiment is repeated for other values of V_{CB} say 1V & 6V etc.

* The emitter current 'I_E' increases rapidly with small increase in emitter-base voltage 'V_{EB}'. It means the I/p resistance is very small.

I/p resistance :- $\left(R = \frac{V}{I}\right)$

It is the ratio of change in emitter-base voltage ΔV_{EB} to the resulting change in emitter current ΔI_E. at constant collector-base voltage V_{CB}.

i.e. $$r_i = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}\ \text{constant}}$$

I/p resistance of is quite small of the order of a few ohms.

O/p characteristics :-

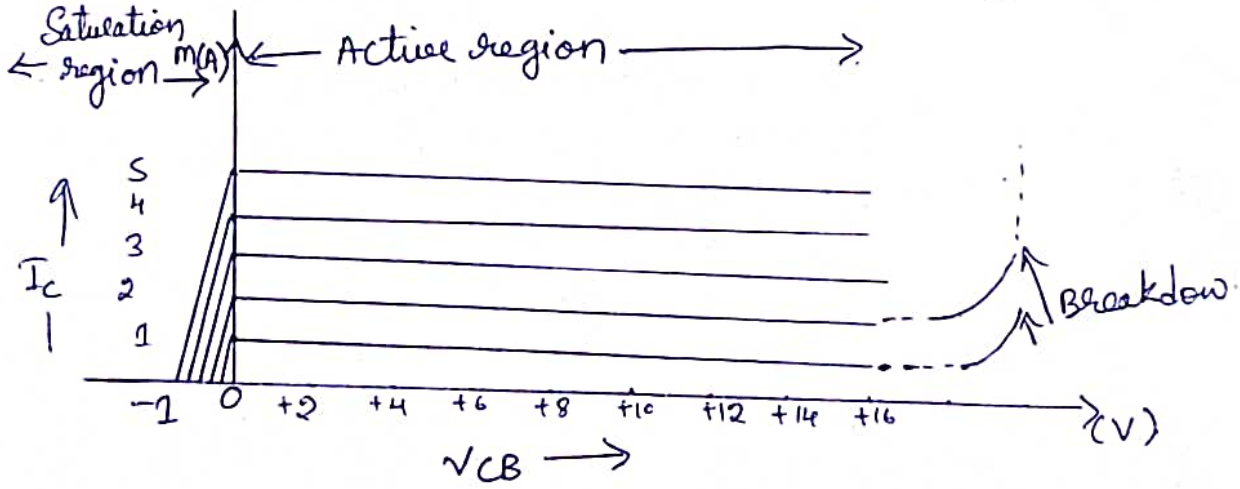
* These curves gives the relationship between the collector current 'I_C' & the collector - base voltage 'V_{CB}' for a constant emitter current 'I_E'.

* Collector current is taken along y-axis & collector voltage along x-axis.

* We have to adjust the emitter - base voltage 'V_{EB}' to get a suitable value of emitter current 'I_E' (say $I_E = 1mA, 2mA$ etc)

* The o/p characteristics is obtained by keeping 'I_E' constant & by noting variation in collector current 'I_C' with variation in collector - base voltage 'V_{CB}'.

* If we plot a graph with collector - base voltage 'V_{CB}' along the horizontal axis & the collector current I_C along the vertical axis, which results fig ⑤ o/p characteristics.



* <u>O/p resistance</u> 'r_o' is defined as the ratio of change in collector - base voltage 'ΔV_{CB}' to the resulting change in <u>collector current</u> 'I_C' at constant emitter current 'I_E'.

$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \Big/ \text{constant } I_E.$$

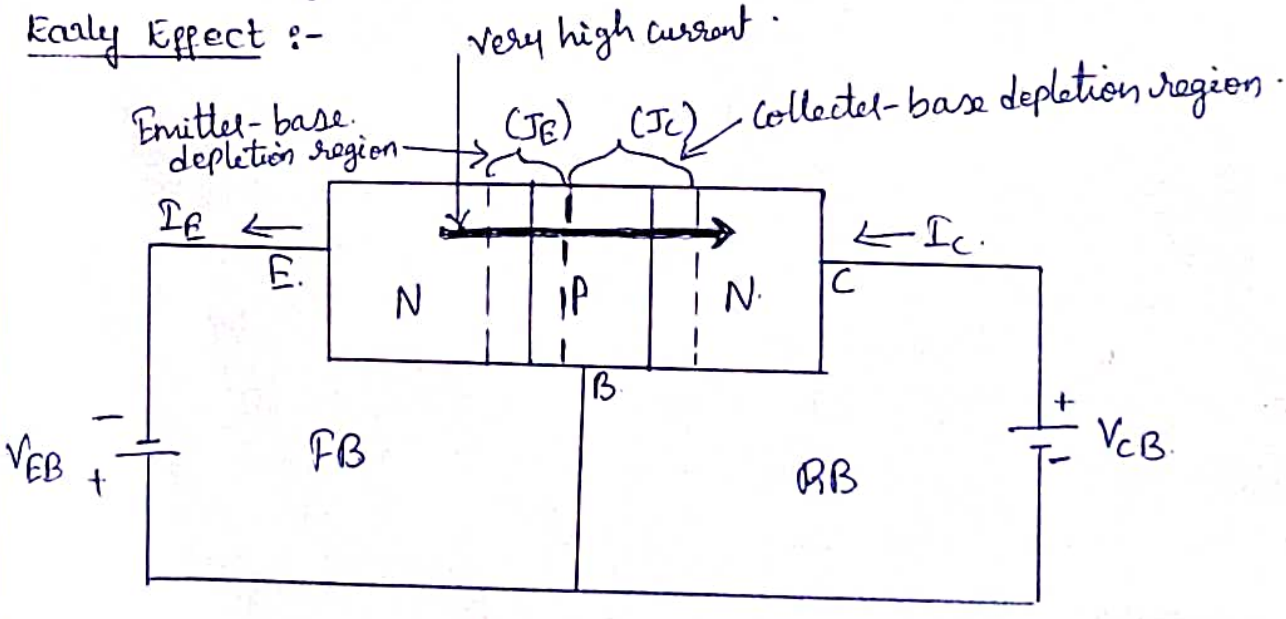
* The o/p characteristic curve is divided into 3 regions namely (i) Saturation region
(ii) Active region
(iii) cutoff region.

i) In saturation region, collector to base voltage 'V_{CB}' is -ve for a NPN transistor. It means that collector - base junction of a transistor is also forward bias in the saturation region. So a small change in V_{CB} results in a large value of 'I_c' current.

ii) In active region, the emitter - base junction 'J_E' is forward bias & collector - base junction 'J_c' is reversed biased. The collector current is constant & is equal to the emitter current. ($I_c \approx I_E$).

iii) In cut-off region, both junctions of a transistor are reverse biased, Hence only a small leakage current flows in the circuit.

Punch - Through effect or Base - width Modulation or Early Effect :-



fig(4): Illustration of Punch through.

* When the reverse bias voltage V_{CB} in the C-B configuration exceeds the maximum values specified by the manufacturer, the collector-base depletion region may penetrate deep into the base until it comes into contact with the emitter-base-depletion region. This condition is called punch through & it as shown in fig (4).

* This leads to the break down of the device & very large currents flow through the device (transistor). The excessive flow of current will damage the transistor.

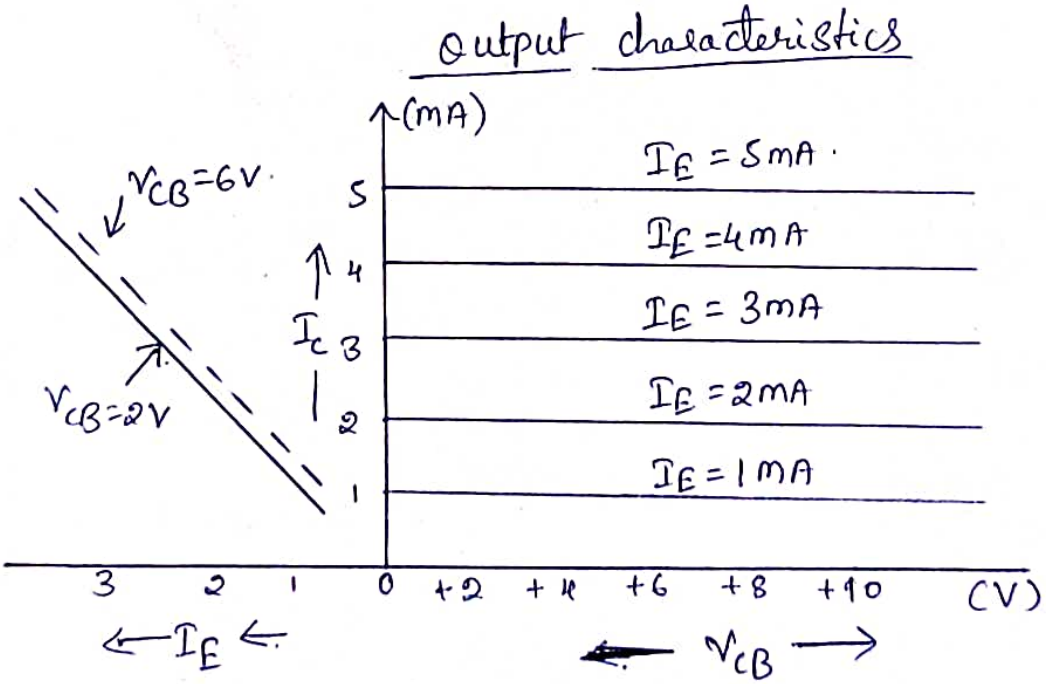
* Maximum values of V_{CB} range b/w 25V & 80V.

Current Gain:-

* The current gain characteristics is also called as forward transfer characteristics.

* It is a plot of the o/p current 'I_C' against variations in I/p current 'I_E' when V_{CB} is held constant.

fig:



Common Emitter Characteristics :- (NPN)

* Draw the input and output characteristics of CE circuit. Explain active, saturation, cut-off region.

June 10, 8M	Jan-03, 9M	Jan-04, 9M	June 04, 6M

* Draw the common emitter circuit. Draw the input & output curves and explain the terms active region, cutoff region and saturation region.

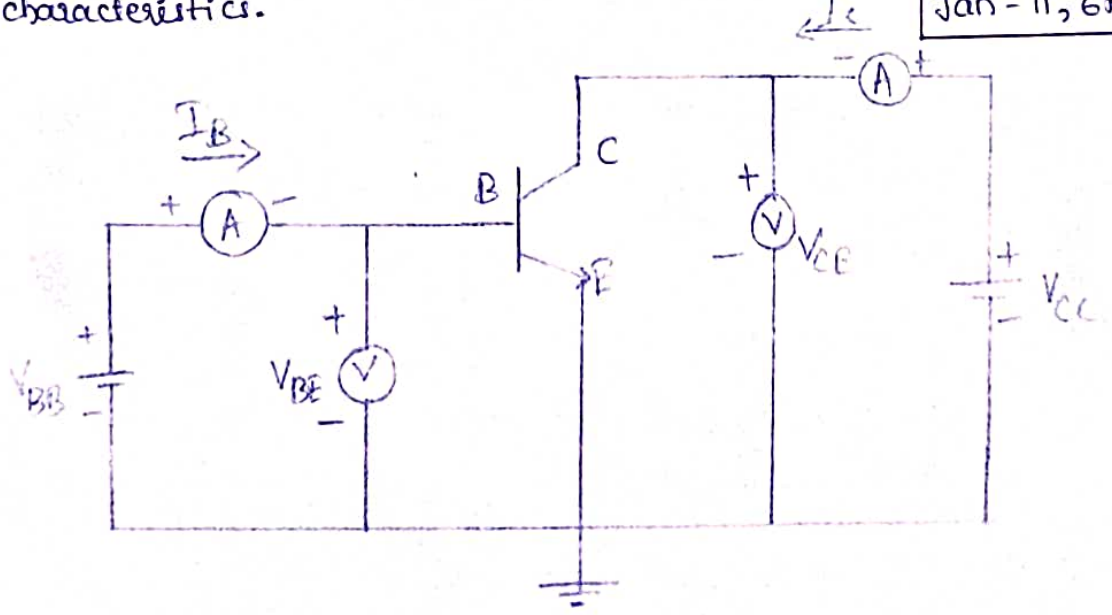
June-09, 8M	June 08, 8M	Jan 08, 7M	June 06, 5M	June 05, 7M

* Draw the input and output characteristics curve of a transistor in common-emitter configuration. Explain their nature and shape. what do their slope represents?

Jan-07, 7M

* Explain the input and output characteristics for a CE configuration BJT circuit. Discuss each region on the characteristics.

Jan-11, 6M (OLD)

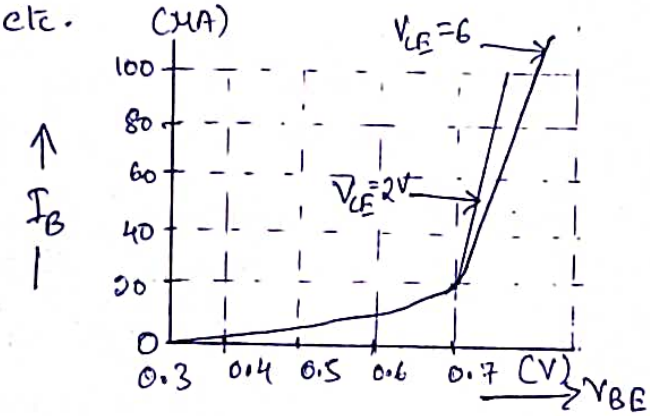


fig① : ckt for determining transistor common emitter characteristics.

* These curves give the relationship b/w the base current I_B & the base emitter voltage V_{BE} for a constant collector emitter voltage V_{CE}.

* To obtain Ilp characteristic, the olp voltage 'V_{CE}' is kept constant, Ilp voltage 'V_{BE}' is varied in small intervals & the corresponding change in Ilp current 'I_B' is recorded.

* I_B is then plotted against V_{BE} as shown in fig ②. The experiment is repeated for other values of 'V_{CE}' say 2V, 6V, ... etc.



* Ilp resistance is defined as the ratio of change in base-emitter voltage 'ΔV_{BE}' to the resulting change in base-current 'ΔI_B' at constant collector emitter voltage.

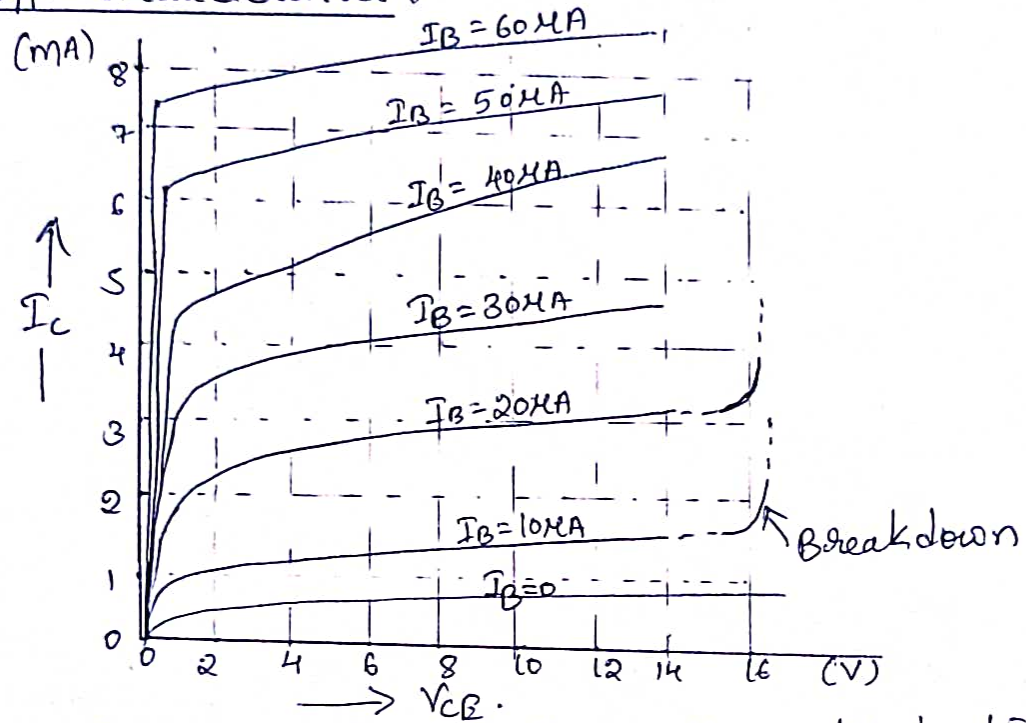
$$R_i = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE}\ \text{constant}}$$

(600Ω to 400Ω)

* fig ② shows that, for a given level of V_{BE}, I_B is reduced when higher V_{CE} levels are employed. This is because higher 'V_{CE}' produces greater depletion region penetration into the base, reducing the distance b/w the CB & EB depletion regions.

* Thus more of the charge carriers from the emitter flow across the CB-Junction & less current flow from base terminal.

O/p characteristics :-



* By using base-emitter voltage 'V_{BE}', 'I_B' is maintained constant at several convenient levels.

* 'V_{CE}' is varied in suitable steps & at each step I_C value is recorded. The same procedure is repeated for different settings of I_B.

* If we plot a graph with 'V_{CE}' voltage along horizontal axis & the collector current 'I_C' along the vertical axis, we shall obtain a o/p characteristics as shown in fig ⑤.

* o/p resistance 'r_o' is defined as the ratio of change in collector to emitter voltage 'ΔV_{CE}' to the resulting change in collector current 'ΔI_C' at constant base current 'I_B'.

$$r_o = \left.\frac{\Delta V_{CE}}{\Delta I_C}\right|_{I_B \text{ constant}}$$

(10KΩ to 50KΩ)

* The o/p characteristics curve is divided into 3 regions namely:

1) Saturation region.
2) Active region.
3) cut-off region.

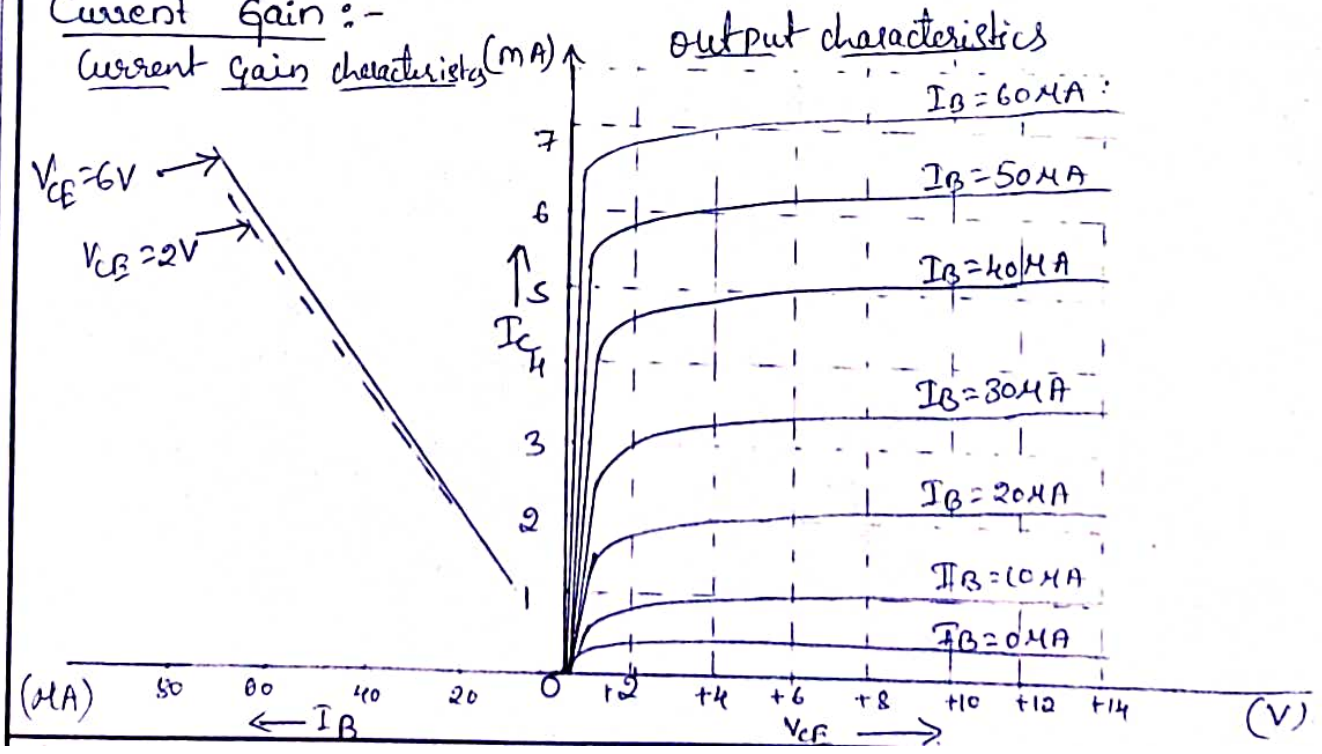
i) In saturation region, when the collector to emitter voltage 'V_{CE}' is increased above zero, the collector current 'I_c' increases rapidly to a saturation value, depending upon the value of base current.

* It may be noted that collector current I_c reaches to a saturation value when V_{CC} is about 0.5V.

ii) In active region, the collector current is β_{dc} times greater than the base current. Thus small I/p current 'I_B' produces a large o/p current I_c.

iii) In cutoff region, when base current is zero ($I_B = 0$), collector current is not zero ($I_c \neq 0$), a small collector current exists called reverse leakage current 'I_{CEO}'.

Current Gain :-



* Common emitter current gain characteristics shows the variation of I_C as a function of I_B with constant 'V_{CE}'. i.e 'V_{CE}' is held at a convenient level & I_B is varied in suitable steps and at each step I_C value is recorded. I_C is then plotted as a function of I_B.

* A vertical line is drawn through a selected V_{CE} value & the corresponding levels of I_C & I_B are read along the line.

Common Collector characteristics :- (NPN)

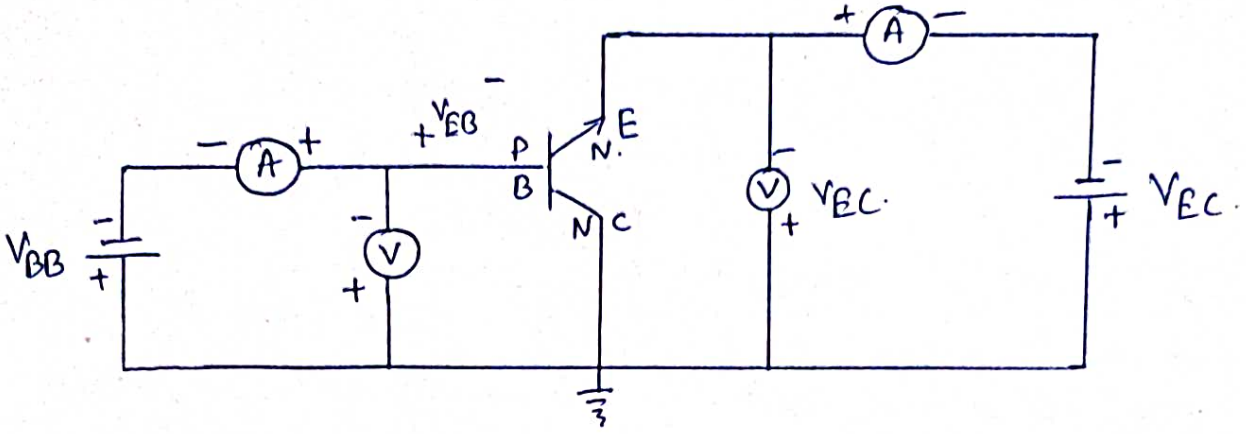


fig ①: circuit for obtaining common-collector characteristics.

I/p characteristics :-

* In common-collector circuit, collector terminal is common to both I/p & o/p terminal.
* Common collector I/p characteristics shows the variation of I_B with V_{BC} at a constant V_{EC}.
* V_{EC} is set to a convenient value. V_{BC} is varied in suitable steps and at each step I_B value is recorded.
* I_B is then plotted against V_{BC} as shown in fig ②. The experiment is repeated for other values of 'V_{EC}' say 3V, 6V etc

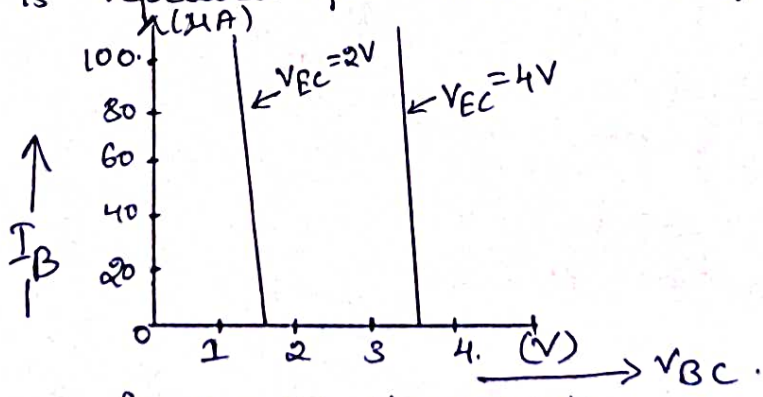


fig ②: I/p characteristics.

* fig ② shows the common collector I/p characteristics. This is quite different from either CB or CE I/p characteristics. The difference is due to the fact that the I/p voltage V_{BC}, is largely determined by the V_{EC} level.

Applying KVL from emitter to base ckt.

$$-V_{EC} + V_{EB} + V_{BC} = 0.$$

$$V_{BC} = V_{BC} - V_{EB} \rightarrow (1)$$

(or)

$$V_{EB} = V_{EC} - V_{BC} \rightarrow (2)$$

* At a constant V_{EC}, if V_{BC} is increased, V_{EB} reduces and as a result I_B decreases.

o/p characteristics :-

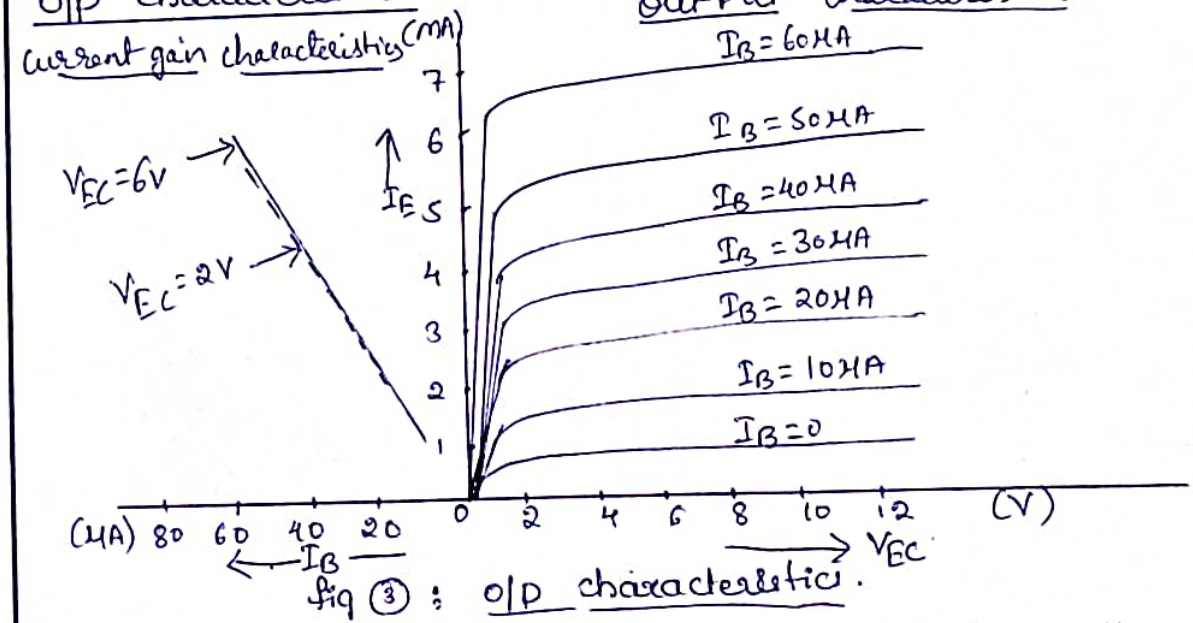


fig (3) : o/p characteristics.

* common-collector o/p characteristics shows the variation of I_E as a function of V_{EC} at a constant I_B.
* I_B is set to a convenient value, V_{EC} is varied in suitable steps and at each step I_E value is recorded. The same procedure is repeated for different settings of I_B.
* the common collector current gain characteristics are I_E plotted versus I_B for several fixed values of V_{CE}.
* The I_C is approximately equal to I_E, the common collector o/p characteristics & current gain characteristics are practically identical to those of the common-emitter circuit.

Comparision of Transistor configurations :-

* Compare various BJT circuit configuration. Jan 11, 4M (OLD)

Sl.NO	Characteristic	Common Base	Common Emitter	Common collector
1	Input Resistance	Very low (100Ω)	Low (1kΩ)	High (500kΩ)
2	Output Resistance	Very high (1MΩ)	High (40kΩ)	Low (50Ω)
3	Input current	I_E	I_B	I_B
4	Output current	I_C	I_C	I_E
5	Input voltage applied between	Emitter and Base	Base and Emitter	Base and collector.
6	output voltage taken between	Collector and Base	Collector and Emitter	Emitter and collector.
7	current amplification factor	$\alpha_{dc} = \frac{I_C}{I_E}$	$\beta_{dc} = \frac{I_C}{I_B}$	$\frac{I_E}{I_B}$
8	Current gain	Less than unity	High (20 to few hundreds)	High (20 to few hundreds
9	Voltage gain	Medium	Medium	less than unity
10	Applications	As a input Stage of Multistage amplifier	For audio Signal amplification	For impedence Matching.